Evaluating DC-DC Converters and PDN with the E5061B LF-RF Network Analyzer

Application Note

Agilent Technologies

Introduction

Switch-mode DC-DC converters/ voltage regulators are widely used in electronic equipment in a variety of industries. One industry that's driving the most recent technical evolutions of DC-DC converters is computer equipment. Here, DC-DC converters play an important role for power integrity (providing a steady Vdd voltage regardless of the load variations) in the power supply circuits called PDNs (power distribution networks); which consist of bare PC board power planes, DC-DC converters, and passive PDN components such as bypass capacitors mounted on the power planes. The most significant trend in PDN of the computer equipment is that the load devices such as MPU's, FPGA's, and ASIC's are continuously evolving toward faster operating speeds and lower operating voltages. Also, various voltage levels are required by these LSI's (3.3 V, 2.5V, 1.5 V, 1.2 V, etc). In accordance with these trends, distributed power architecture is becoming common, where the low-voltage DC-DC converters are mounted at the point-of-load (POL) to improve the power integrity in high performance computer systems (i.e. servers and network infrastructure equipment). To make the DC-DC converters quickly respond to load variations of high-speed LSI's, it is more important than ever to optimize the balance of the response speed and the stability of the feedback loop circuits. To minimize the transient voltage fluctuations due to large load current variations and ensure the voltage is maintained within narrower margins of the low voltage systems, it is necessary to verify that the output impedance of the DC-DC converter is suppressed to an extremely small value of milliohm order. In addition, PDN designers need to evaluate the impedance of passive PDN components such as bypass capacitors up to high frequencies beyond the DC-DC converter's loop bandwidth, where the passive PDN components suppress the impedance between the power and ground planes. Accurately knowing the characteristics of each passive PDN component helps improve the quality of PDN design using simulation tools. Also, by measuring the entire PDN impedance of the PC board after mounting the passive components, we can verify if the desired target impedance is achieved as simulated. In general, the frequency range of interest is up in the hundreds of MHz range, which is an upper limit frequency for suppressing the PDN impedance with on-board passive components.

This application note describes the measurement methods for evaluating the frequency domain characteristics of DC-DC converters and associated passive PDN components by using the E5061B-3L5 LF-RF network analyzer with Option 005 impedance analysis function (5 Hz to 3 GHz). The first part of this document discusses how to measure feedback loop characteristics of DC-DC converters. The second part discusses impedance measurements of DC-DC converters and the passive PDN components.

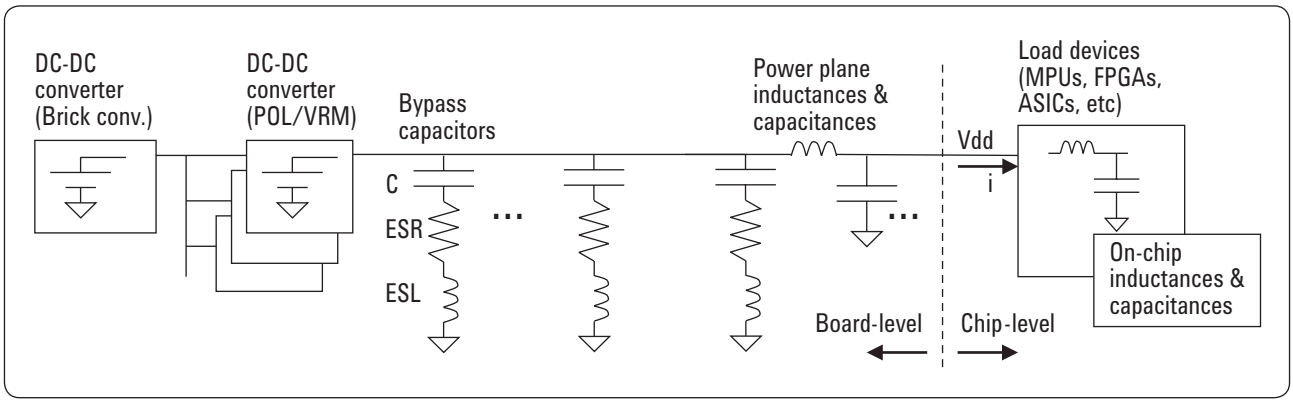

Figure 1. Example of power distribution network

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Evaluating Feedback Loop Characteristics of DC-DC Converters

DC-DC Converter Basic Theory of Operation

First of all, let's quickly summarize the basic theory of operation of the DC-DC converter. The example shown here is a simple non-isolated single-phase buck converter with a voltage-mode control.

The block diagrams and the timing charts shown in Figure 2 explain the basic operation of a buck DC-DC converter. The input DC voltage Vin is converted to pulsed voltage with a switch (MOSFET). It's on/off condition is controlled by the feedback loop circuit, the pulsed voltage is converted to the output DC voltage Vout with the charging and discharging operations of the output LC filter.

When the switch is turned on, the current Ion flows through the inductor L and the power is delivered to the output capacitor Cout and the load, then Vout is increased.

If Vout reaches a certain voltage level, the switch is turned off and the energy that was charged to L by the current Ion generates the current Ioff and delivers the power to the load together with the energy that was charged to Cout, then Vout is decreased. If Vout reaches a certain level, the switch is turned on and Vout is increased again. The output voltage level is determined by the pulse duty ratio.

The longer the period Ton, the higher the output voltage. The shorter the period Ton, the lower the output voltage. When a current higher than a certain level continuously flows through the inductor L, the averaged output voltage is calculated as Vout = Ton/(Ton + Toff) x Vin. By repeating this on/off operation while monitoring the output voltage and adjusting the pulse duty ratio, the regulated output DC voltage is obtained regardless of the load variations.

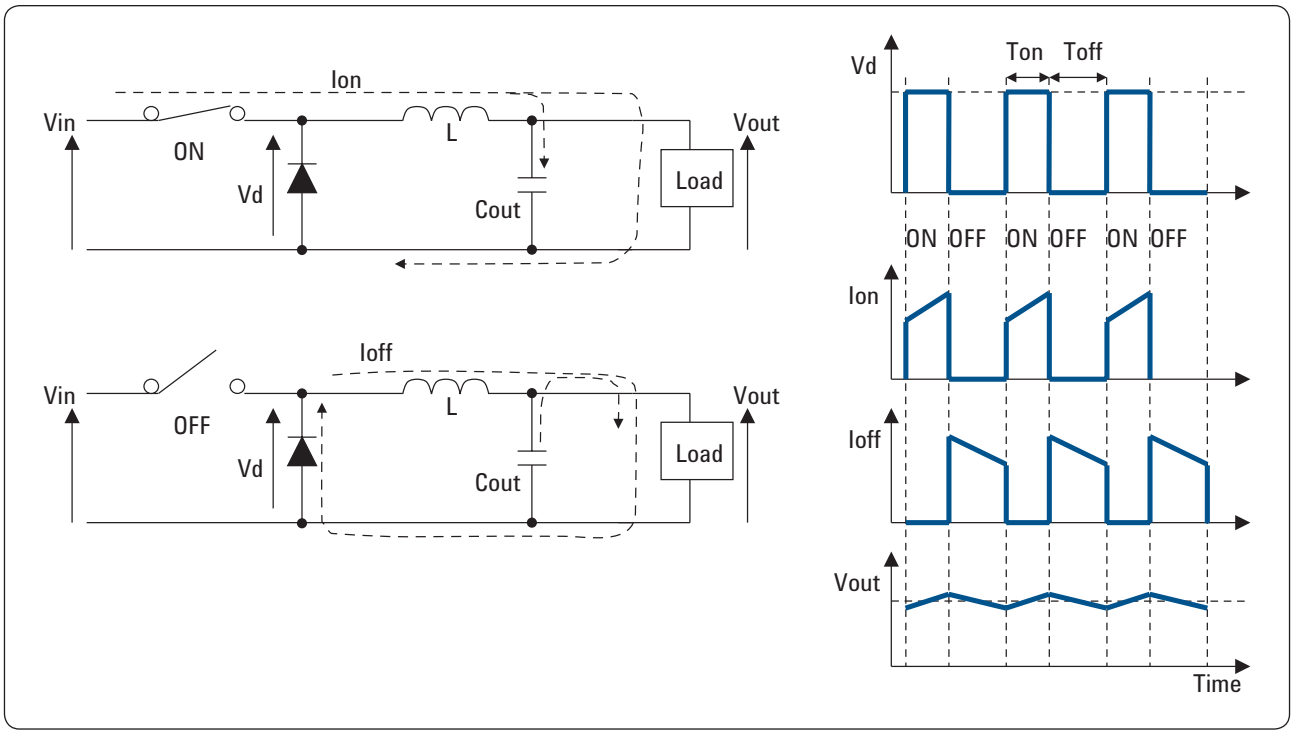


Figure 2. DC-DC converter basic theory of operation

Figure 3 shows an example of a detailed converter block diagram. The output voltage divided by R1 and R2 is fed back to the error amplifier; the error amplifier compares the feedback voltage with the stable reference voltage Vref to provide the output voltage proportional to the difference between them. The pulse width modulator (PWM) provides the pulse with the duty ratio determined by the error amplifier's output voltage and the pulse turns the MOSFET on and off.

When the feedback voltage is lower than Vref, the feedback system extends the period Ton to increase the output voltage. When the feedback voltage is higher than Vref, the feedback system shortens the period Ton to decrease the output voltage. Thus the regulated DC output voltage is obtained.

C1, C2, C3, R3, and R4 are the components which adjust the gain and phase delay of the error amplifier to improve the feedback loop stability (feedback compensation) together with R1 and R2.

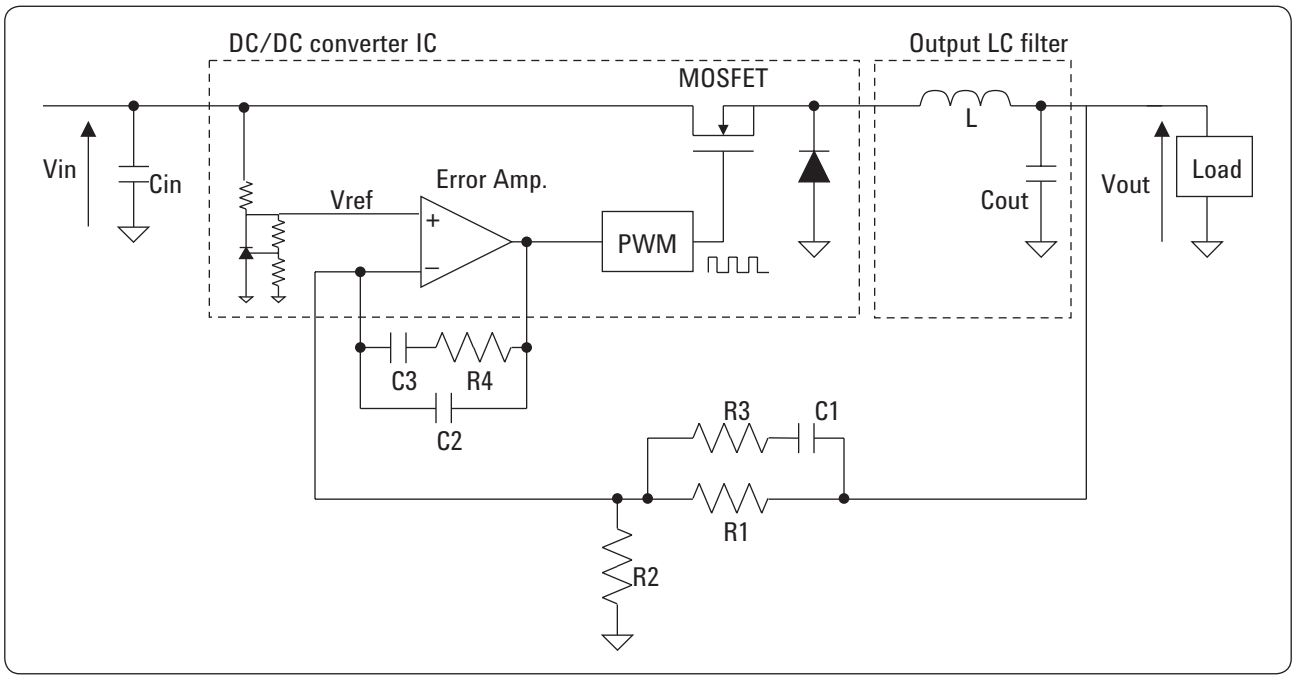


Figure 3. Example of DC-DC converter block diagram

Evaluating feedback loop characteristics of DC-DC converters

This section describes how to evaluate the feedback loop characteristics with the E5061B-3L5 LF-RF network analyzer. Before starting the discussion on the measurement methods, we quickly summarize the basics of the feedback loop control.

Loop gain

As shown in Figure 4, the DC-DC converter can be regarded as a negative feedback control system, which has the input signal Vref and the output signal Vout. |G| is called the open loop gain, |Vout/Vref| = |G/(1 + GH)| is called closed loop gain, and |GH| is called loop gain. It should be noted that the round transfer function is GH x (-1) = -GH because it includes the inversion at the error amplifier. The transfer function G corresponds to the total transfer function from the error amplifier to the output LC filter, and transfer function H corresponds to the resistive divider circuit that consists of R1 and R2. The resistors R1 and R2 also determines the gain and phase delay of the error amplifier, together with R3, C1, C2, C3, and R4.

This negative feedback control system regulates the varying output voltage Vout closer to Vref/H. The larger the loop gain |GH|, the better the voltage regulation. As the frequency of the variation increases, the loop gain decreases and as the loop gain becomes lower than 1, the regulation will not work.

The frequency where the loop gain |GH| is equal to 1 (= 0 dB) is called the crossover frequency, which indicates the bandwidth of the loop (Figure 5). The higher crossover frequency enables the feedback loop to regulate the voltage variation of higher frequencies and the response speed to the load variations becomes faster.

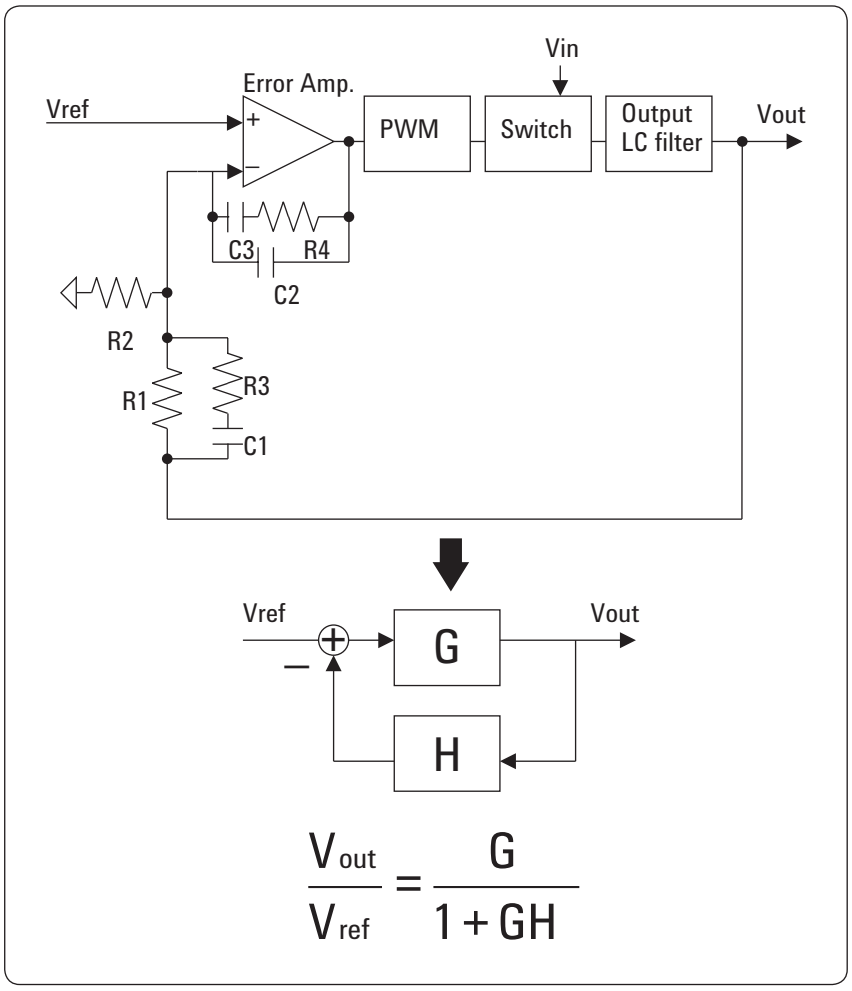


Figure 4. Negative feedback loop control system

Phase margin and gain margin

The phase delay occurs at high frequencies. Now let's look at the phase delay of the round transfer function -GH. In the low-frequency range near DC, only the 180° phase delay of the error amplifier occurs. As the frequency progresses higher, the phase delay of the error amplifier gets larger and additional delays occur at other locations in the loop. As shown in Figure 6, the large phase delay occurs around the resonant frequency fc = 1/(2*pi*sqrt (L*C)) of the output LC filter. Especially in the case of low-ESR capacitors that are widely used for reducing the output ripple noise, the LC filter's phase response becomes close to the ideal LC filter's due to the extremely low ESR, and the phase delay around the resonant frequency becomes very large, close to 180°. If the total phase delay of the feedback loop is close to 360°, the feedback loop will appear as positive feedback, rather than the negative feedback. If the loop gain |GH| is still more than 1, an unstable control loop is likely to cause oscillation due to the variation of the components used in the loop circuits and other environmental changes such as temperature.

To avoid this problem, the feedback compensation for stabilizing the loop is implemented, adjusting the gain and phase of the error amplifier around the resonant frequency of the LC filter by adding the feedback compensation components (R3, R4, C1, C2, and C3 in Figure 4). As shown in Figure 5, the difference between the phase angle of -GH and -360° at the crossover frequency where the loop gain |GH| = 1 (that is, the difference between the phase angle of GH and -180°) is called the phase margin. The phase margin is an important parameter that shows the loop stability. The larger the phase margin, the more stable the feedback loop.

The feedback loop must have enough phase margin to ensure the stable operation under any load condition of the actual application.

However, if the crossover frequency becomes low as a result of excessive feedback compensation, the response speed to the load variations will be slower. Therefore, it is necessary to design the feedback compensation circuits so that the stability and the response speed are optimized for the requirements of targeted applications. To optimize these parameters, validating the actual loop characteristics with the low-frequency network analyzer is crucial.

Similarly, the difference between the gain of -GH and 0 dB at the frequency where the phase is 0° is called the gain margin, which is also the key parameter for evaluating the loop stability.

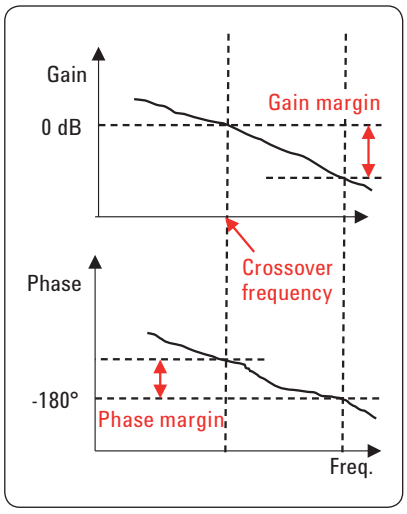


Figure 5. Gain-phase characteristics of GH

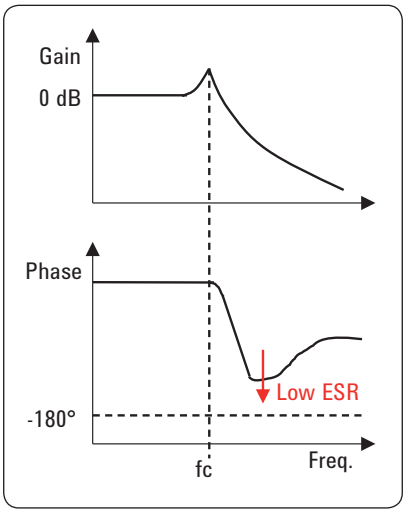


Figure 6. Gain-phase characteristics of output LC filter

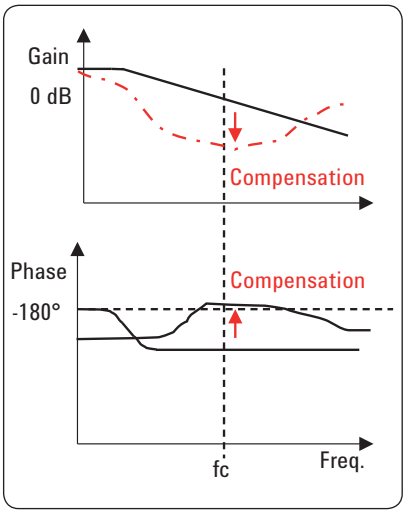


Figure 7. Gain-phase characteristics of error amplifier block and feedback compensation

Loop gain measurement method with network analyzer

The feedback loop circuit in its operating condition can be measured with a low-frequency network analyzer by injecting the analyzer's source signal into the feedback loop via an additional injection circuit. The analyzer measures the ratio of the AC voltages at both ends of the injection circuit with the receiver ports R and T that have high impedance inputs. The signal should be injected at the point where the input impedance Zin is high and the output impedance Zout is low.

In the case of the DC-DC converters, the test signal is generally injected at the point just before the divider circuit on the feedback path by using the floating injection circuit that consists of a transformer and a resistor, as shown in Figure 8. By injecting the test signal at the point where Zin >> Zout is satisfied and using the resistor R that satisfies Zin >> R >> Zout, we can measure the round transfer function -GH with the ratio measurement T/R without disturbing the original loop characteristics.

The injected signal level should not be very high to prevent the feedback loop circuit from getting into the nonlinear region. The probing should be done with the high input impedance as not to affect the operation of the feedback loop circuit.

As for the measurement frequency range, it's common that the measurement is started from the low frequencies like 10 Hz or 100 Hz. But in general, the important frequency range for evaluating the loop characteristics of DC-DC converters is typically several kHz to several hundreds of kHz where the LC filter's resonant frequency and the loop crossover frequency exist. Therefore, the measurement at the low-frequency range does not have to be so strict.

Note that the measurement method discussed here is basically applicable to the linear voltage-mode control loops only. It is not applicable to the current-mode control loops and nonlinear control loops.

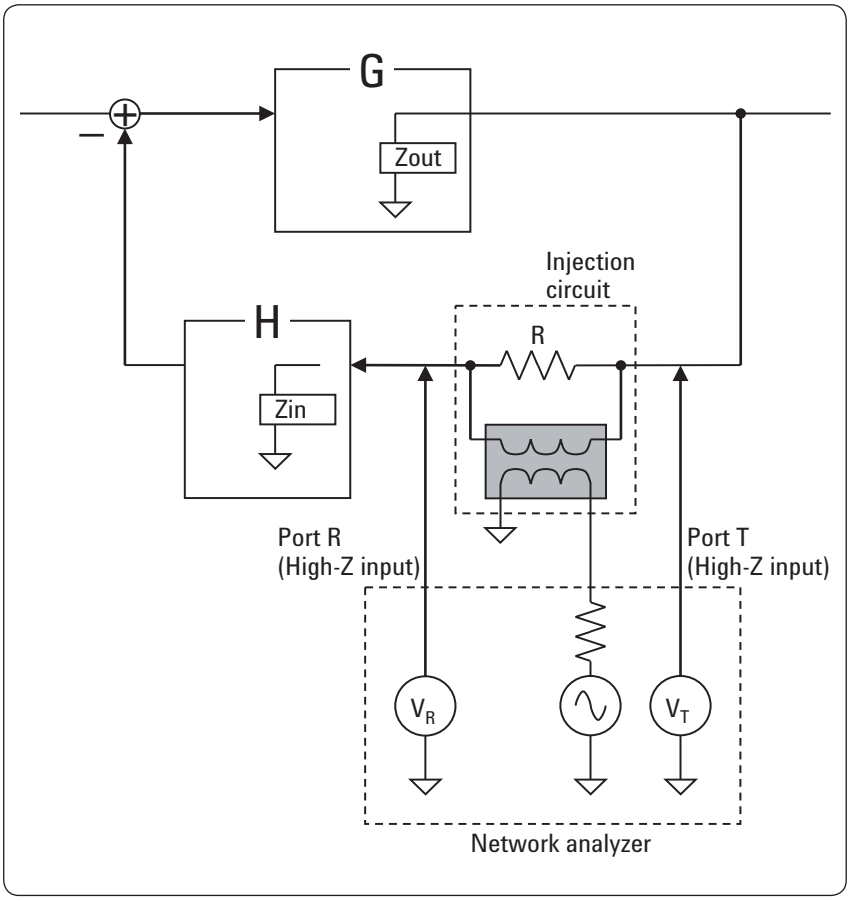


Figure 8. Loop gain measurement method for negative feedback control systems

Configuration example of loop gain measurement

Figure 9 shows a configuration example for measuring loop gain by using the gain-phase test port of the E5061B-3L5 LF-RF network analyzer. The gain-phase test port provides the 1 MΩ/50 Ω switchable direct receiver inputs with a frequency coverage of 5 Hz to 30 MHz.

The transformer T1 and the resistor R5 configure the floating signal injection circuit. The resistance value of R5 should be sufficiently smaller than Zin, which is generally several kohms or several tens of kohms. Also, if the resistance of R5 is too small, the injected test signal will be excessively attenuated. Around 20 to 100 ohm is widely being used, but lower resistance like 5 ohm may improve the transformer bandwidth, depending on the transformer to be used.

The receiver ports R and T are set to the 1 MΩ input mode (input impedance Zin = 1 MΩ//30 pF). The coaxial test leads are used for connecting the ports R and T to the DUT. It is recommended to use the coaxial test leads rather than the 10:1 passive probes for this loop gain measurement configuration, because both the source and receiver ports are floated from the DUT's ground in this configuration, and the 10:1 passive probe might cause measurement errors associated with stray coupling. (Note that the ports R and T are semi-floated from its chassis ground with the floating impedance of about 30 Ω, as described in Figure 22.) A relatively larger probing capacitance of the coaxial test leads is not a problem because the required frequency range for this measurement is generally no more than 1 MHz, and we can obtain high enough probing input impedance even with the coaxial test leads. If you use the 10:1 passive probes in this measurement configuration with the floating source injection, it is recommended to connect the outer shield of the LF OUT port (the analyzer's chassis ground) to the DUT's ground via a short lead, as shown with the dotted line in Figure 9.

For the load of the converter, a DC electronic load or high power resistors are generally used.

To calibrate the measurement system, perform the response through calibration to eliminate the differences in the amplitude and the phase between two test leads by contacting them to the point TP1.

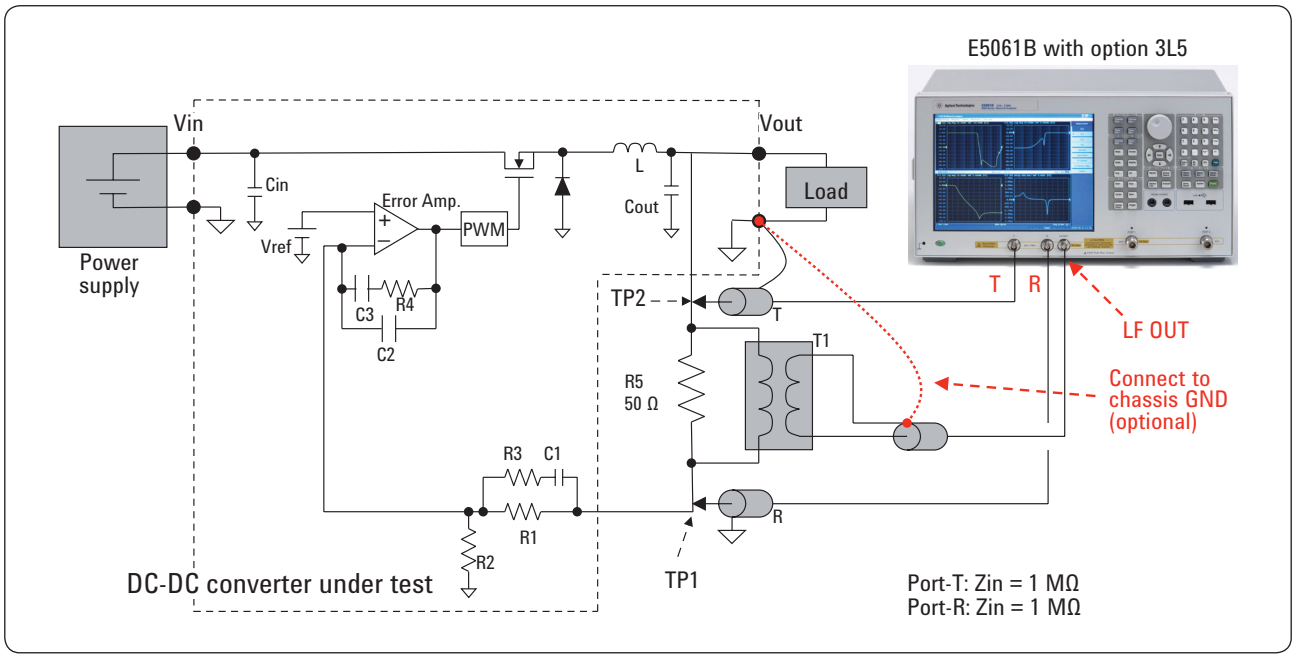


Figure 9. Configuration example for measuring loop gain

Measurement example of feedback loop characteristics

Figure 10 shows a loop gain measurement example of a 5 V-to-3.3 V buck converter with 2 ampere load by using the measurement configuration shown in Figure 9. The measurement frequency range is 100 Hz to 1 MHz, the source level is -20 dBm. The IFBW is set to AUTO mode (100 Hz limit), which automatically selects narrow IFBW at low frequencies and wider IFBW at higher frequencies. The upper graph shows the loop gain, and the lower graph shows the phase response. The peak response nearby the stop frequency is caused by the switching noise of the DC-DC converter itself.

The marker is placed on the crossover frequency (about 30 kHz). In this measurement example, the analyzer measures the round transfer function -GH. The phase measurement value at the crossover frequency (about 80°) indicates the phase margin. The converter measured in this example has enough phase margin and it seems possible to improve the response speed to the load variations by further tuning the feedback compensation circuits to make the crossover frequency higher.

Injection signal level

Now we assume that the constant floating AC voltage is injected at the resistor R5, which is in the secondary side of the injection transformer regardless of the test frequency range. This floating AC voltage is divided into two AC voltages referenced to the DUT's ground at the receiver ports R and T according to the loop gain at each frequency point. In the low-frequency range where the loop gain is high, the small AC voltage appears at port R, and the large AC voltage appears at port T. As the frequency increases, the AC voltage at port R increases, and the AC voltage at port T decreases. At the crossover frequency where the loop gain is 0 dB, the same level of the AC voltage appears at ports R and T.

As for the injection signal level, it is generally desired to inject a large AC signal in the low-frequency range where the AC voltage that appears at port R becomes low and the measurement SNR tends to worsen.

However, doing so will make the feedback loop circuit get into the nonlinear region in the middle frequency range around the crossover frequency, because the AC voltage level entering into the error amplifier becomes too large. Therefore, the injection signal level should be set to an appropriate level that is not too large and not too small.

To choose the appropriate signal level, first set the analyzer's source level to a sufficiently low level (e.g. -20 or -30 dBm) and perform the measurement. Repeat the measurements while increasing the source level gradually, and then choose the source level that is slightly lower than the level where unusual behaviors such as discontinuous waveforms start to appear. Also, if necessary, check the signal level by monitoring the absolute power at the port T, in addition to the ratio measurement T/R. Confirm that the measured power level at the port T is linearly increased in the source ranges you are selecting, or monitor the signal waveforms in the feedback loop circuits with an oscilloscope and confirm that the waveforms are not distorted.

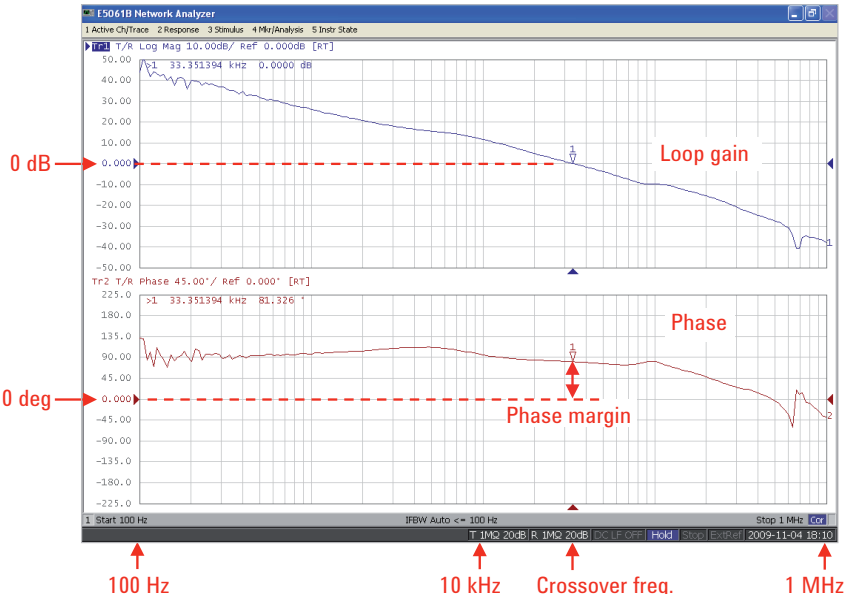


Figure 10. Loop gain measurement example of DC-DC converter

Setting variable injection levels with segment sweep

Some DC-DC converters may require a very low injection signal level, as low as -30 dBm or less. In this case, the measurement trace in the low-frequency range will be rather noisy. It is not critical for evaluating the loop stability by looking at the measurement trace in the middle frequency range around the crossover frequency. However, if you want to improve the measurement SNR in the low-frequency range while not applying an excessive injection signal in the middle frequency range, a possible solution is to make a logarithmic frequency sweep table with gradually decreasing source settings from high to low levels. Figure 11 shows a loop gain measurement example by injecting the following signal levels according to the frequency range by using the segment sweep function:

-10 dBm at 100 Hz to 500 Hz
-15 dBm at 500 Hz to 1 kHz
-20 dBm at 1 kHz to 3 kHz
-25 dBm at 3 kHz to 5 kHz
-30 dBm at 5 kHz to 10 kHz
-35 dBm at 10 kHz to 1 MHz

The sweep table used in this measurement example consists of 201 segments with a single measurement point, and the IFBW of each segment is set to about 1/5 of the test frequency. The segment table can be edited on the external PC as a CSV file and imported into the analyzer, or it is possible to make the segment sweep table by using the analyzer's built-in VBA programming function. Note that the grid of the graph is deleted by modifying its color setup because the equally-spaced X-axis grid is displayed in the segment sweep mode, which is confusing for the logarithmic frequency plots. You can access the display color setup menu by pressing [System], (Misc Setup), (Display Setup), and (Color setup) keys.

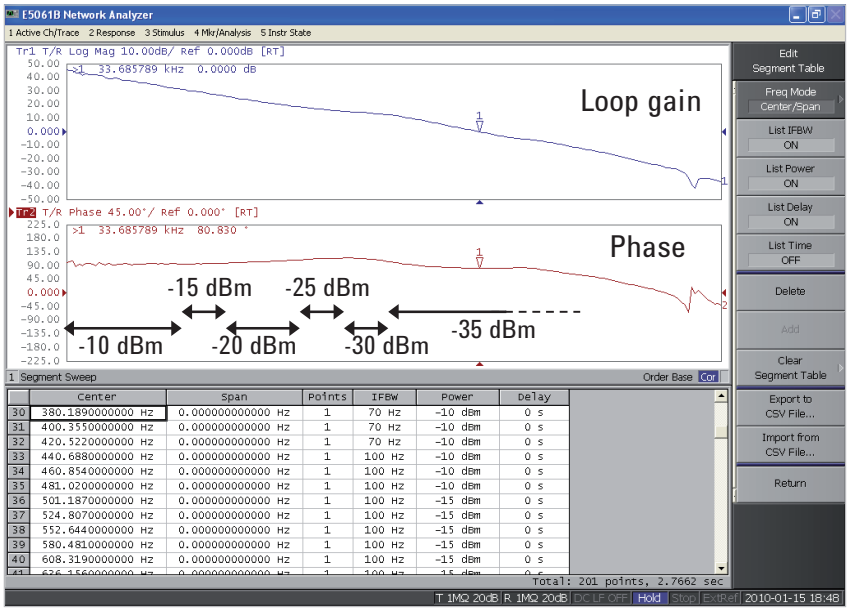


Figure 11. Setting variable injection level with segment sweep

How to select injection transformer

Select the injection transformer with a flat transmission response in the entire test frequency range. The transformer should have an impedance that is not extremely smaller than the analyzer's source output impedance of 50 Ω, which means the self inductance L should be large enough. Also, the transformer must work properly in the high-frequency region without making a self resonance. In the measurement example shown in Figure 10, the source signal was injected with the 1:1 pulse transformer (Agilent PN 5188-4425, self inductance 3.4 mH) in combination with a 50 Ω resistor as R5.

Figure 12 shows the S21 transmission response of this pulse transformer in the 50 Ω system impedance, which is measured with the S-parameter test port of the E5061B-3L5. The measurement frequency range is 10 Hz to 10 MHz. As shown in the marker readings, the transformer gives a flat response in the high-frequency range up to more than 1 MHz. On the other hand, in the low-frequency range around 100 Hz, 20 dB loss occurs because the transformer's impedance |Z| = |j*2*pi*f*L| is lower than the analyzer's source output impedance 50 Ω, and the AC voltage applied to the primary side of the transformer becomes very small. This causes further disadvantages in terms of the measurement SNR because the 20 dB loss of the transformer is added on top of the originally small AC level due to the high loop gain in the low-frequency range.

Figure 13 shows the absolute AC voltage measurement results at ports R and T by using the same configuration as the loop gain measurement shown in Figure 10 (source level = -20 dBm fixed). Note that the measured AC voltage Vac is indicated as 20*Log (Vac^2/50), although the input impedance of the R and T ports is not 50 Ω but high impedance.

As you can see, the measured level around 100 Hz is very low because of these two factors. If you use the 10:1 passive probes instead of the coaxial test cables, the measured AC voltage at port R will be lower and the measurement SNR at 100 Hz will be worse due to the probe's 20 dB loss. However, the important frequency range for evaluating the feedback loop is generally around the crossover frequency, and the trace fluctuation in the low-frequency range is not a problem.

To improve the loop gain measurement SNR in the low-frequency range when applying a fixed source level (especially if the DUT requires a very low injection level), use the transformer that has a flat response down to the low-frequency range. The primary recommendation is the Picotest J2100A Injection Transformer which is optimized for this application (1 Hz to 5 MHz with R5=5 ohm, 10 Hz to 5 MHz with R5=50 ohm, BNC(f) to banana jacks, **www.picotest.com**). Note that the pass band insertion loss will be about 15 dB when terminated with R5=5 ohm. Or another transformer applicable to this application is the North Hills 0017C 50 ohm Video Isolation Transformer (10 Hz to 5 MHz with R5=50 ohm, BNC(f) to BNC(f), **www.northhills-sp.com**).

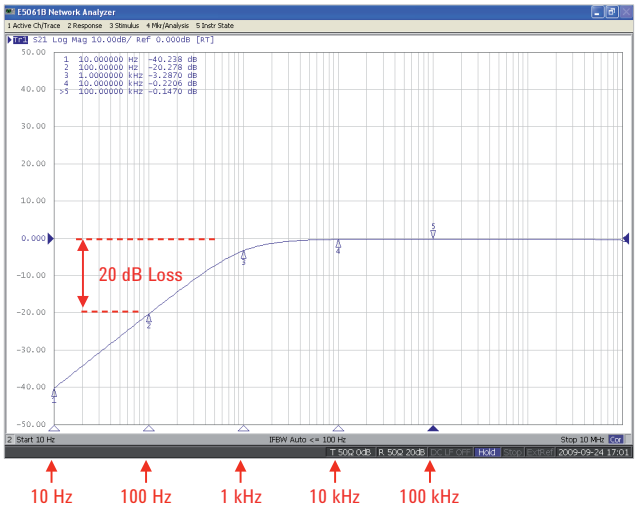


Figure 12. Transmission characteristic of pulse transformer (PN 5188-4425)

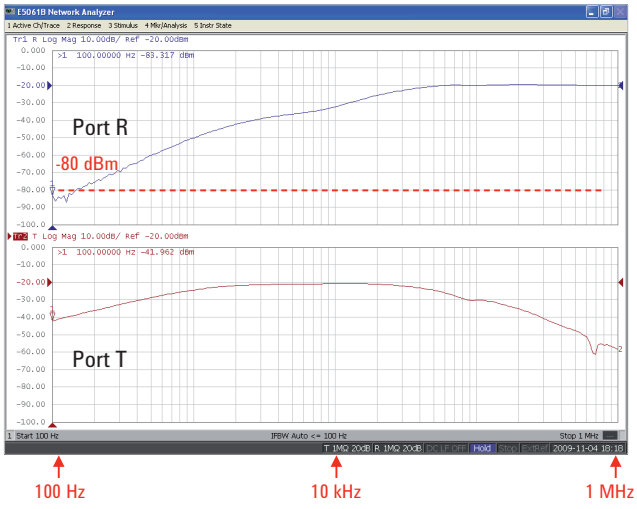


Figure 13. Absolute AC voltage measurements in the loop gain measurement configuration (Source level = -20 dBm fixed)

Evaluating Impedance of DC-DC Converters and Passive PDN Components

Evaluating output impedance of DC-DC converters

It is getting important to evaluate a very small impedance of the PDNs for the recent low-voltage LSIs where the large current flows. Here, if we assume Zpdn is the impedance between the Vdd and ground planes that is seen from the load devices and Delta-I is the current variation caused by the operation of the load devices, the voltage drop Delta-V = Delta-i x Zpdn will occur in the power plane. More strictly speaking, the voltage drop will be:

Delta-V = IFFT(FFT(delta-I) x Zpdn). [1]

In the case of high-performance LSIs such as MPUs, Delta-I can be several amperes or several tens of amperes, and the voltage drop Delta-V will not be negligible. This may cause signal integrity problems and EMI problems. To prevent this, it is necessary to suppress the power plane impedanceZpdn to a small value in the broad frequency range from DC to GHz.Especially in the low-frequency range, an extremely small impedance of milliohm order is often required.

The DC-DC converter provides this very small impedance in the low-frequency range. Regulating the converter's output voltage with the feedback loop control regardless of any load variation equivalently means that very small output impedance is actively achieved. The relationship between the output impedance and the loop gain is given as Zclosed = Zopen/(1+GH), where Zopen is the open-loop output impedance, Zclosed is the closed-loop output impedance, and GH is the loop gain. The closed-loop output impedance will be very small in the low-frequency region where the loop gain is high.

To evaluate the output impedance of the DC-DC converter, we directly measure the closed-loop output impedance Zclose by probing the output terminals of the DC-DC converter by using the low-frequency network analyzer. This section describes how to measure the output impedance of the DC-DC converters by using the E5061B-3L5 LF-RF network analyzer with Option 005 impedance analysis function.

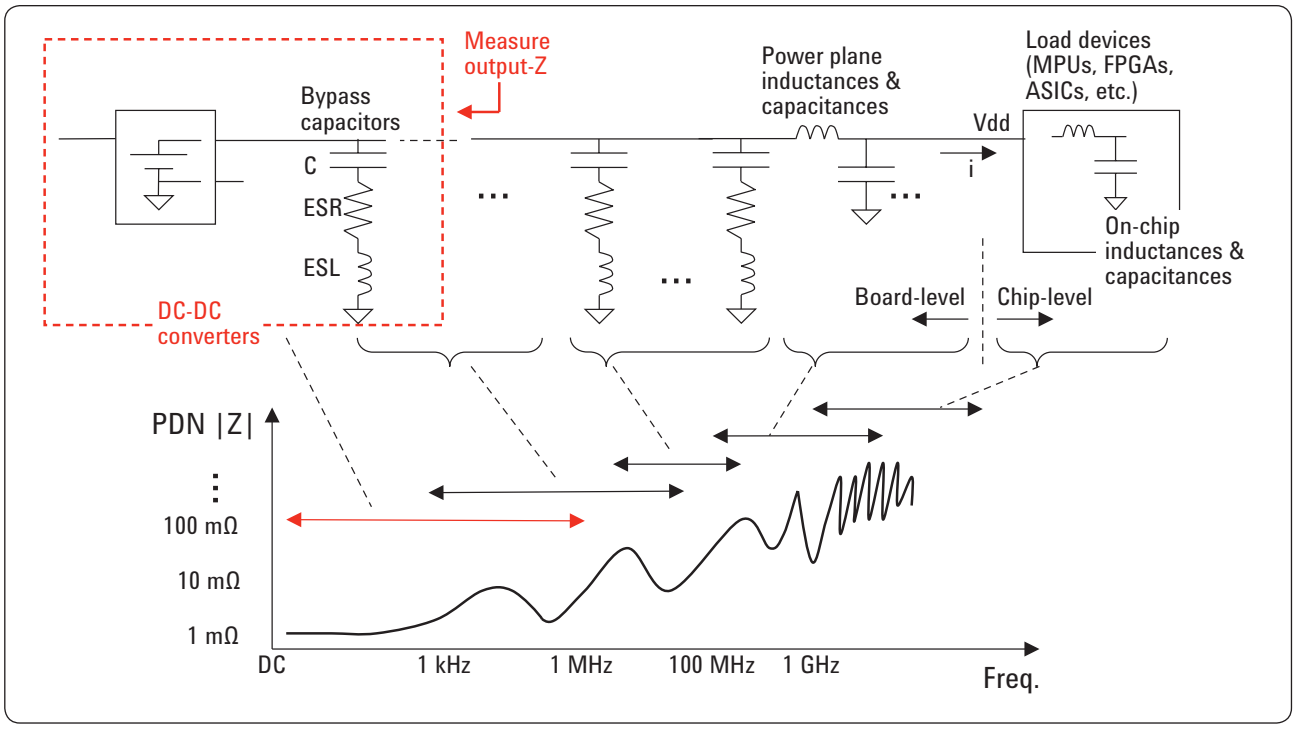


Figure 14. DC-DC converter output impedance in PDN

Current-voltage detection method

This method has traditionally been used for evaluating the output impedance of the DC-DC converters and switch-mode power supplies. Figure 15 shows a simplified block diagram. By floating the network analyzer's signal source with the transformer, the AC voltage and current at the grounded DUT can be measured with the network analyzer's high-impedance inputs. The port T detects the AC voltage Vdut across the DUT, and the port R detects the AC voltage across the 1 Ω resistor, which is equivalent to the AC current Idut that flows through the DUT. The measured voltage ratio T/R directly indicates the DUT's impedance because of the equation T/R = Vdut/(1 x Idut). The DUT in this figure corresponds to the DC-DC converter and the load connected to it.

Similarly to the loop-gain measurement, an electronic load or a high-power resistor are generally used as the load. The analyzer actually measures the parallel impedance of the DC-DC converter and the load, but generally the output impedance of the DC-DC converter is dominant because it is much smaller than the load impedance. The blocking capacitor prevents the DUT's DC output from flowing into the transformer and the 1 Ω resistor. Its impedance |Z| = |1/(j*2*pi*f*C)| should be sufficiently small to obtain a good measurement SNR in the low-frequency range.

This measurement method is suitable for testing the DC-DC converters of relatively high-output voltages because the source is well isolated from the DUT's output DC voltage and the receivers are connected with robust high-impedance inputs. Also, the measurement error associated with the test cable ground loop does not occur because the source is floated with the transformer (described later). However, as it is difficult to fully eliminate the measurement error caused by the residual impedance around the connection of the 1 Ω resistor, this method is not suitable for precisely measuring the very small impedance of mΩ order.

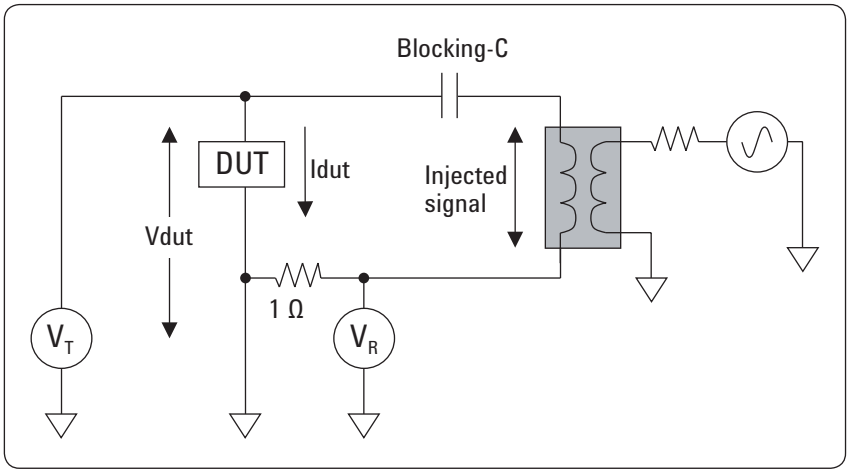


Figure 15. Current-voltage detection method

Configuration example of current-voltage detection method

Figure 16 shows a configuration example of the current voltage detection method by using the gain-phase test port of the E5061B-3L5. For the transformer T1, you can use the same pulse transformer that was used for the loop gain measurement. However, the off-the-shelf isolation transformers designed for use with 50 Ω or 75 Ω system impedance, such as the North Hills model 0017C, are not recommended for this measurement method, because it seems an unwanted residual response is likely to occur if these transformers are used in this measurement configuration.

A blocking capacitor is used for preventing the DC current from flowing through the transformer's winding and the 1 Ω resistor. A large electrolytic capacitor is used for sufficiently injecting a source signal in the low-frequency range.

The current sensing 1 Ω resistor should be as precise as possible. By measuring the impedance of the resistor itself, you can do compensation using simple math. For example, if the impedance of the resistor is 0.98 Ω, you can obtain the DUT impedance Zdut by multiplying the measured impedance Zmeas with 0.98, because Zmeas is calculated as Zmeas = T/R = Vdut/(Idut x 0.98) = Zdut/0.98. If you use a lead resistor, make its lead length as short as possible, and it should be directly soldered to the DUT's output terminal to minimize the measurement error due to the lead residual impedance and the contact resistance between the resistor and the DUT. To measure the small AC voltage at the port T with a good SNR, its internal attenuator should be set to 0 dB, and the source output level should be set to the maximum level 10 dBm. To calibrate the measurement system, perform the response thru calibration by connecting the test cable of the port T to the same point as the port R. When performing the through calibration, reduce the source level to below -5 dBm not to overload the port T receiver.

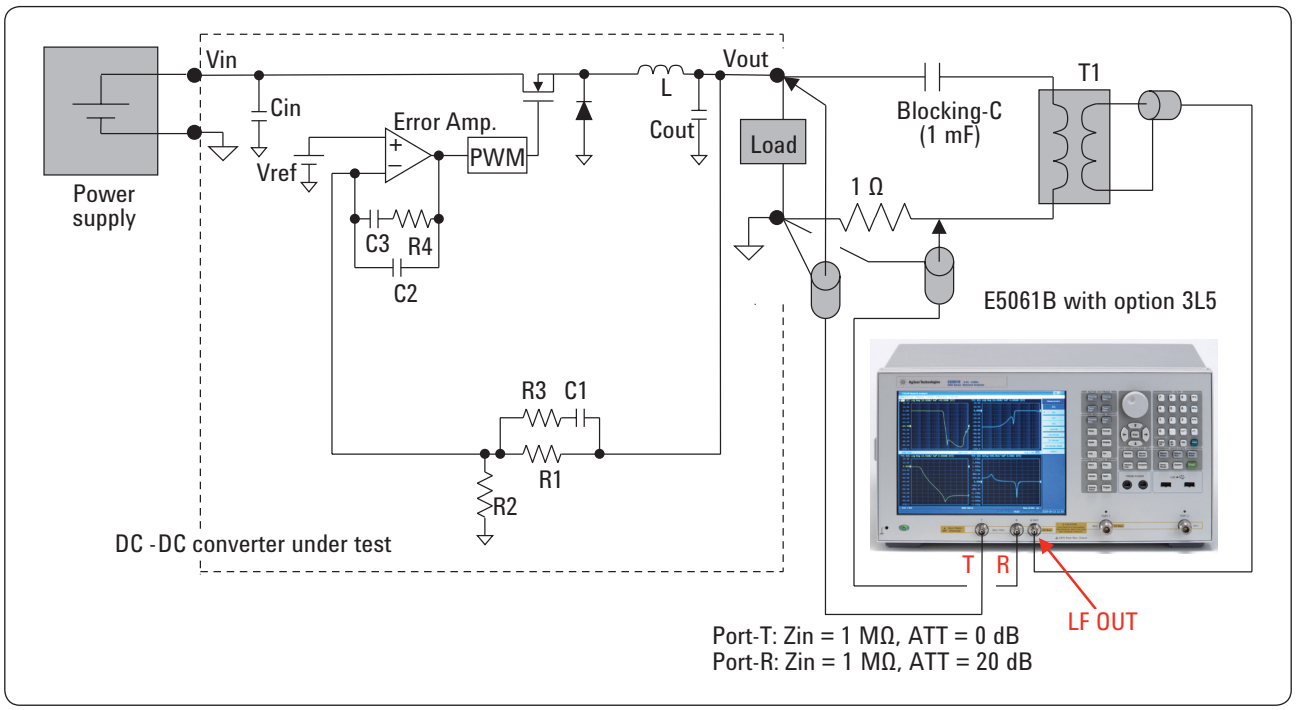


Figure 16. Configuration example of current-voltage detection method

Shunt-thru method

The measurement method that provides more accurate mΩ impedance measurements is the shunt-thru method. The shunt-thru method provides good measurement sensitivity in the impedance range below 50 Ω down to the very small impedance range. It is commonly used for PDN impedance measurements. Figure 17 shows a simplified block diagram. The transmission coefficient S21 is measured by connecting the DUT in the shunt connection between the signal line and the ground. The impedance is derived from S21, which indicates a high attenuation caused by the small shunt impedance. The relation between the DUT's impedance Zdut and S21 is given as Zdut = 25 x S21/(1-S21).

Measurement error caused by test cable ground loop [1] [2] [3]

It is difficult for conventional low-frequency network analyzers with grounded receivers to measure a mΩ shunt impedance in the low-frequency range, because the measurement error is caused by the test cable ground loop between the source and receiver.

Now we assume that the DUT's impedance Zdut is close to 0 Ω. In the block diagram of Figure 18, the voltage V_o is almost zero and the voltage V_T measured at the receiver should also be almost zero. However, since the source current flows into the cable's outer shield of the V_T receiver side as shown in the doted line, the voltage drop V_{C2} occurs across the cable shield resistance R_{C2} and the measured voltage V_T will be V_{C2}, which is incorrectly higher than the voltage V_o that we want to measure. Consequently, the measurement dynamic range is degraded and the measured impedance cannot be lower than R_{C2} even when Zdut is 0 Ω. R_C is generally 10 or a few tens of mohms depending on the swaging quality of the cable shield to the connectors, thickness of the cable shield, cable length, and so on.

Generally, this problem occurs in the low-frequency range below 100 kHz, which is an essential frequency range for evaluating the impedance of DC-DC converters and bulk bypass capacitors. In the higher-frequency range, this problem does not occur because the shield current that flows into the V_T receiver side is blocked with the reactance of the cable shield itself (X = 2*pi*f*L) that is increased along with the frequency.

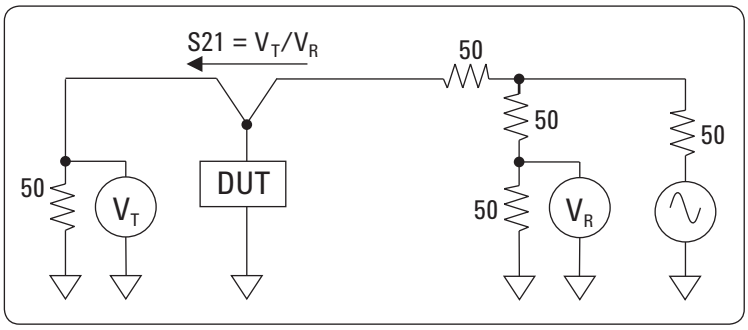


Figure 17. Shunt-thru measurement method

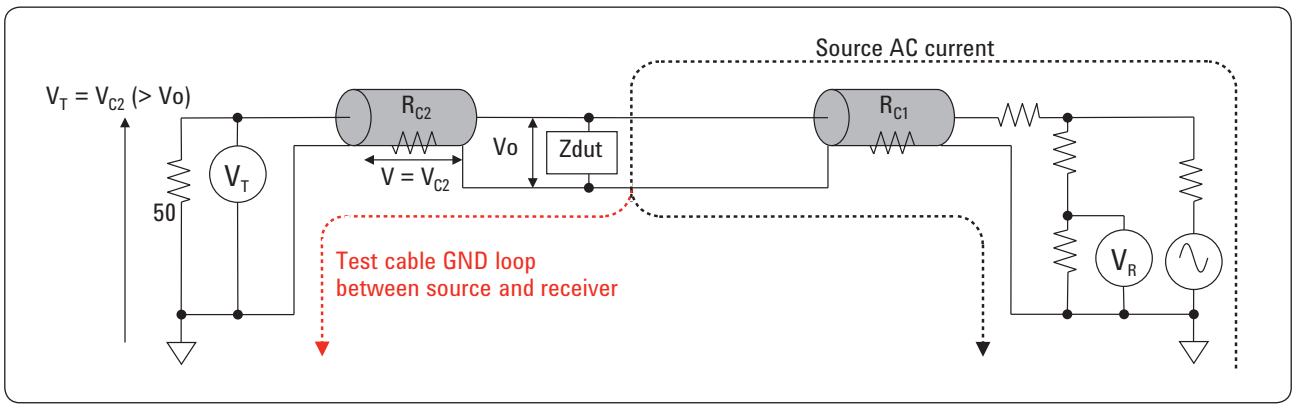


Figure 18. Measurement error due to test cable ground loop

Conventional solutions -1

There are several techniques to minimize this measurement error by using external devices.The most traditional approach is to attach magnetic cores with a large inductance to the coaxial test cable at either of the source side or receiver side (or at both sides). The equivalent circuits of attaching the magnetic cores to the coaxial test cables are shown in Figure 19 and 20. The impedance of the magnetic core suppresses the AC current that flows only through the center conductor or the outer shield, while not suppressing the AC current that goes through the center conductor and returns through the outer shield. When the core is attached to the V_T receiver side as shown in Figure 19, the shield current flowing to R_{C2} is suppressed with the impedance caused by the self inductance |Z| = 2*pi*f*L2 and more current will return to the source shield path. Similarly, when the core is attached to the source side as shown in Figure 20, more current will return to the source shield path, because the total impedance consisting of R_{C1}, R_{C2}, and L1′ (the inductance caused by the total magnetic field generated by the forward and return currents) will be smaller if more current is returned to the source shield path rather than the shield path of the V_T receiver side.

To fully suppress the shield current flowing to the V_T receiver side down to the very low-frequency range, it is necessary to clamp multiple high-permeability magnetic cores to the coaxial test cables, or to use a high-permeability toroidal core and turn the coaxial test cable several times around the core to increase the shield impedance as much as possible. However, it is not so easy to find an appropriate core and eliminate the measurement error down to the very low-frequency range.

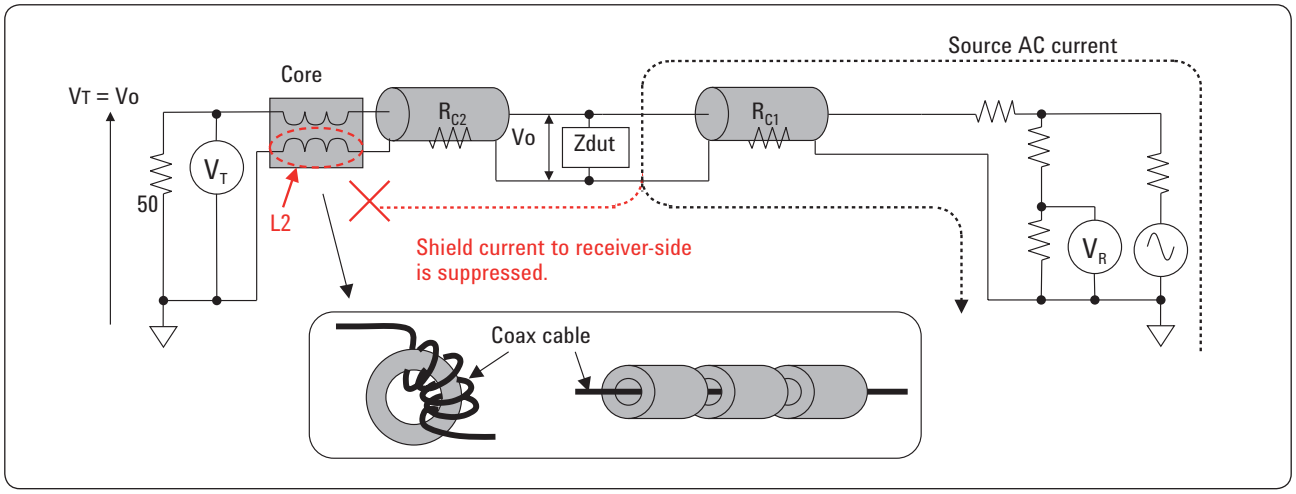


Figure 19. Solution with magnetic core (at receiver side)

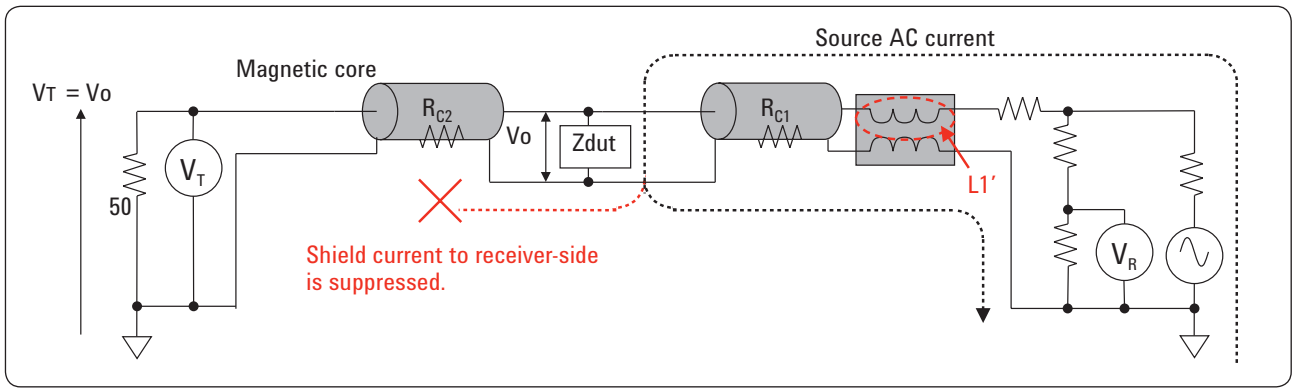


Figure 20. Solution with magnetic core (at source side)

Conventional solutions -2

Another approach is to float the ground of the source or receiver to break the source-to-receiver ground loop. We can implement this by using an isolation transformer or a differential probe. Figure 21 shows a block diagram of connecting an isolation transformer at the source side. The blocking capacitor must be connected between the DUT and the isolation transformer to prevent the DC current from flowing into the transformer. You can use an off-the-shelf broadband 50 Ω isolation transformer such as the North Hills Model 0017C, which can also be used for injecting test signals in the loop-gain measurements.

The isolation transformer is a more effective solution than the magnetic cores in terms of breaking the test cable ground loop between the source and receiver. But the potential side-effect is that the isolation transformer may cause small residual responses in the high-frequency range, depending on the transformer's characteristics. This may not be negligible if the DUT has wide loop bandwidth and exhibits very small impedance up to the high-frequency range.

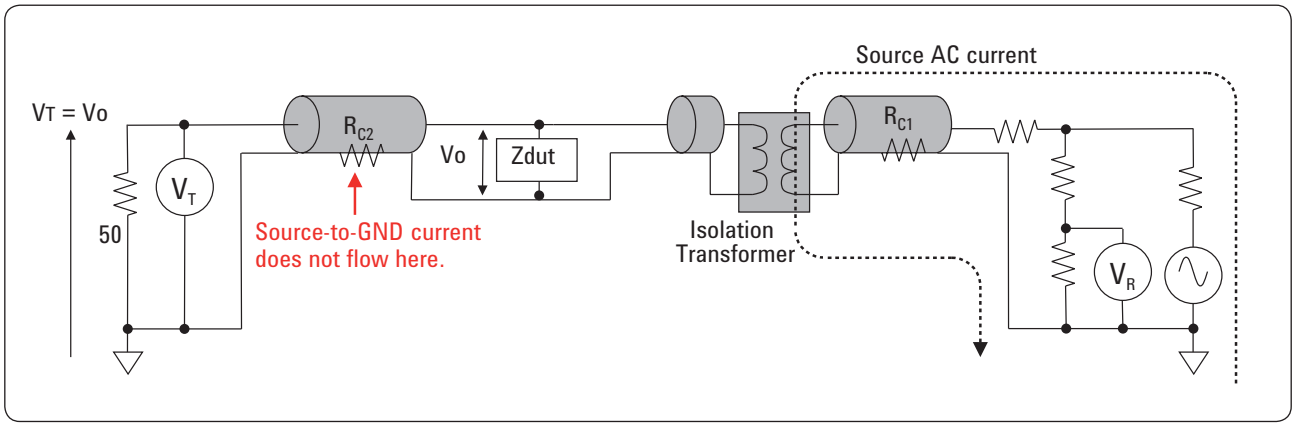


Figure 21. Solution with isolation transformer

Solution with E5061B-3L5

The gain-phase test port (5 Hz to 30 MHz) of the E5061B-3L5 has a unique hardware architecture that enables you to eliminate the measurement error due to the source-to-receiver test cable ground loop. Figure 22 shows a simplified block diagram when using the gain-phase test ports of the E5061B-3L5 for this application. The receivers are semi-floated with the impedance |Zg|, which is about 30 Ω in the low-frequency range below 100 kHz. Similarly to the case of using the magnetic core, we can intuitively understand that the shield current is blocked with the impedance |Zg|. Or if we assume that the voltage swing at the DUT's ground side is Va as shown in Figure 22, since R_{C2} is much smaller than the receiver input impedance 50 Ω, V_T is approximately derived as follows [4],

$$V_T = V_{C2} + V_o$$
$$= Va \times R_{C2}/(R_{C2} + Zg) + Vo$$

Since Rc << |Zg|, the first term of the above equation is negligible, so V_T will be almost equal to Vo and that's what we want to measure. Thus the DUT's impedance can be correctly measured by minimizing the effect of R_{C2}. The gain-phase test port of the E5061B-3L5 enables you to easily measure the DC-DC converter's mΩ output impedance without using an external magnetic core or an isolation transformer.

On the other hand, the S-parameter test port (5 Hz to 3 GHz) of the E5061B-3L5 has grounded-receiver architecture like most of existing low-frequency network analyzers. If you want to measure the DC-DC converter's output impedance of mΩ range with the S-parameter test port (for example, when you want to measure the PDN impedance from low frequencies and up more than 30 MHz in a single sweep), it is necessary to connect magnetic cores to the test cables.

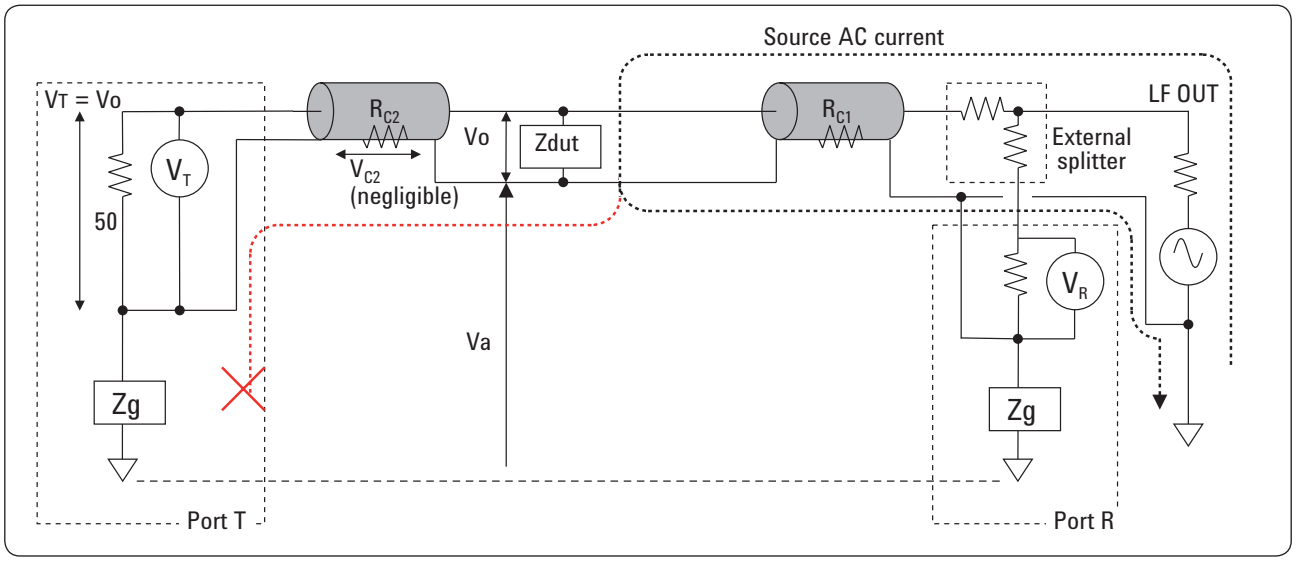


Figure 22. Solution with E5061B-3L5 gain-phase test port

Experimental measurements with short device

Now let's look at simple measurement examples that show the measurement error caused by the source-to-receiver test cable ground loop and the effectiveness of the E5061B's gain-phase test port. The device measured in these examples is a shunt-short device with a lead wire soldered to the SMA receptacles in the shunt connection as shown in Figure 23. This short device is connected to the analyzers via good-conditioned 60 cm BNC cables and SMA-BNC adapters. Figure 24 and 25 show S21 (attenuation) measurement results by using the 4395A and the S-parameter test port of the E5061B-3L5, without magnetic cores or isolation transformers. As you can see, the attenuation measurement traces in the low-frequency range is incorrectly higher than the true value of the DUT in both cases. These errors are due to the test cable ground loop between the source and receiver, as described in Figure 18.

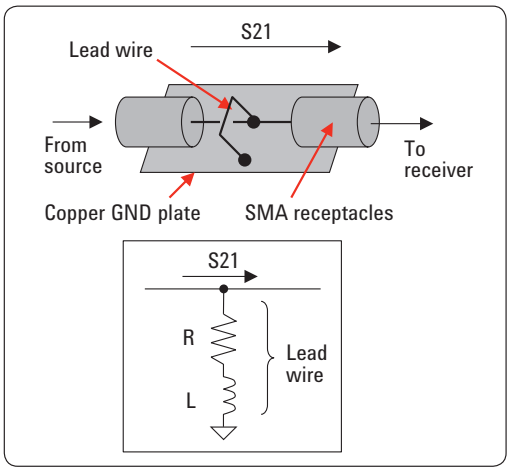


Figure 23. Test device

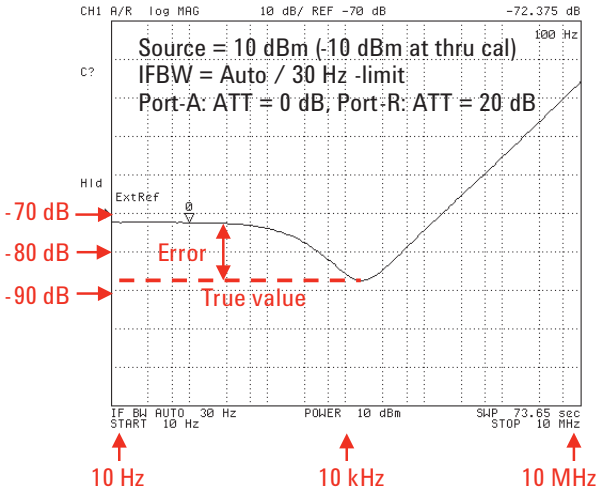


Figure 24. S21 measurement result with 4395A (without core or isolation transformer)

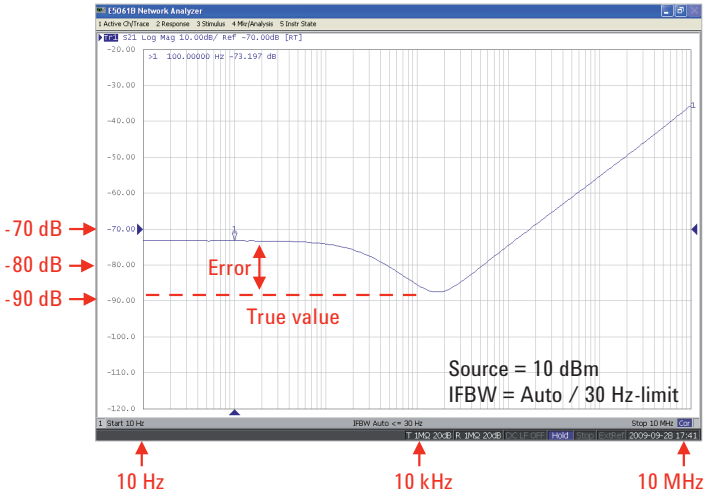


Figure 25. S21 measurement result with S-parameter test port of E5061B-3L5 (without core or isolation transformer)

Experimental measurement with short device, continued

Figure 26 shows measurement results of the same device by using the E5061B-3L5's S-parameter test port with magnetic cores. All the measured traces are stored into the memory traces. The traces measured in the channel-1 are S21 traces, and the traces measured in the channel-2 are |Z| traces. (In this measurement example, the |Z| traces are plotted with the E5061B's shunt-thru impedance conversion function.)

Trace (a) shows the measurement results without cores. Trace (b) shows the measurement results by attaching a clamp-on-type ferrite core (commonly used for noise suppression of interface cables) to the coaxial test cable of the source side. The measurement data is slightly improved but not enough at all for measuring the milliohm impedance down to the low-frequency range, because the impedance generated by such a small core is too small. Traces (c) shows the measurement results by attaching a large toroidal core (Metglas Finemet F7555G, Φ79 mm, **www.metglas.com**), to the test cable of the source side. The measurement trace in the low-frequency range is considerably improved. And trace (d) shows the measurement results by turning the test cable three times to the same toroidal core to significantly increase the impedance generated by the core. Now the correct measurement results obtained down to about 100 Hz.

On the other hand, Figure 27 shows the measurement results by using the gain-phase test port of the E5061B-3L5 without using cores or isolation transformers. As you can see, the correct measurement results are obtained down to the low-frequency range even without using cores or transformers.

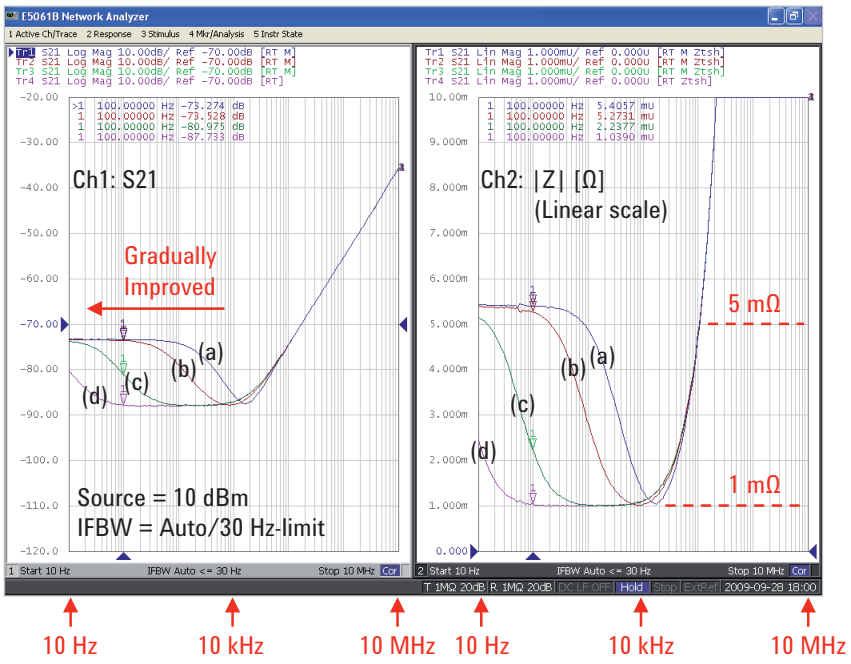


Figure 26. S21 and |Z| measurement results with S-parameter test port of E5061B-3L5

(a) Without core
(b) A clamp-on-type core is attached to test cable.
(c) A large toroidal core is attached to test cable.
(d) Test cable is turned three times around a large toroidal core.

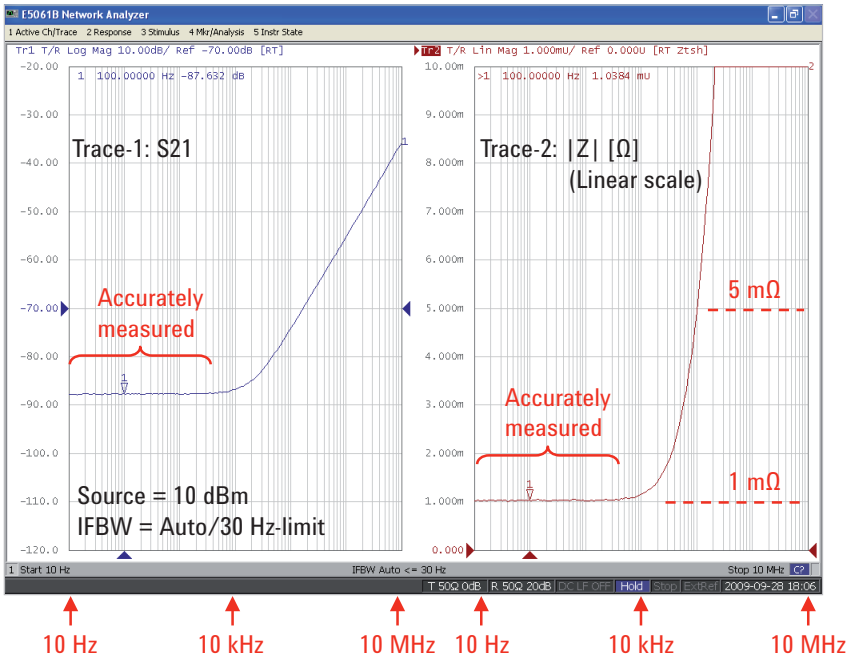


Figure 27. S21 and |Z| measurement results with gain-phase test port of E5061B-3L5

Without core or isolation transformer
Source = 10 dBm (-5 dBm at thru cal)
Port-T: ATT = 0 dB, Zin = 50 Ω, Port-R: ATT = 20 dB, Zin = 50 Ω

Configuration example of shunt-thru method

Figure 28 shows a configuration example of the shunt-thru method with the gain-phase test port of the E5061B-3L5. As described before, it is not necessary to use magnetic cores or an isolation transformer when measuring the mΩ shunt impedance with the gain-phase test port. The input impedance of the receiver ports R and T must be set to 50 Ω. To measure S21 with the gain-phase test port, the source output from the LF OUT port must be separated with an external 2-resistor type power splitter such as the 11667L (DC to 2 GHz, BNC type).

The configuration shown in Figure 28 can measure the DC-DC converters whose output voltage is below about 5 Vdc without using external DC blocking capacitors. In this case, however, note that the DC current flowing into the power splitter and the analyzer's 50 Ω test ports will affect the DUT's loading condition if the load current is not so high.

If a DC voltage higher than 5 Vdc is applied to the gain-phase test port with 50 Ω system impedance, the overload protection function works and the E5061B's test port will be shut-down. To measure the DUT whose output voltage is more than about 5 Vdc, it is necessary to connect external DC blocking capacitors as shown in Figure 28.

To calibrate the measurement system, perform the response through calibration at the end of the test cables. To measure a very small AC voltage at the port T with a good SNR, the IFBW should be set to a narrow value and the internal attenuator should be set to 0 dB. Also, the source output level should be set to the maximum level, 10 dBm. Since the DUT's impedance is much smaller than the analyzer's source output impedance of 50 Ω, excessive signal level is not applied to the DUT even if the source level is set to high. Note that the source level should be reduced to -5 dBm if you perform the through calibration, not to overload the port T receiver with 0 dB attenuator setting. Then after the through calibration, increase the source level to 10 dBm.

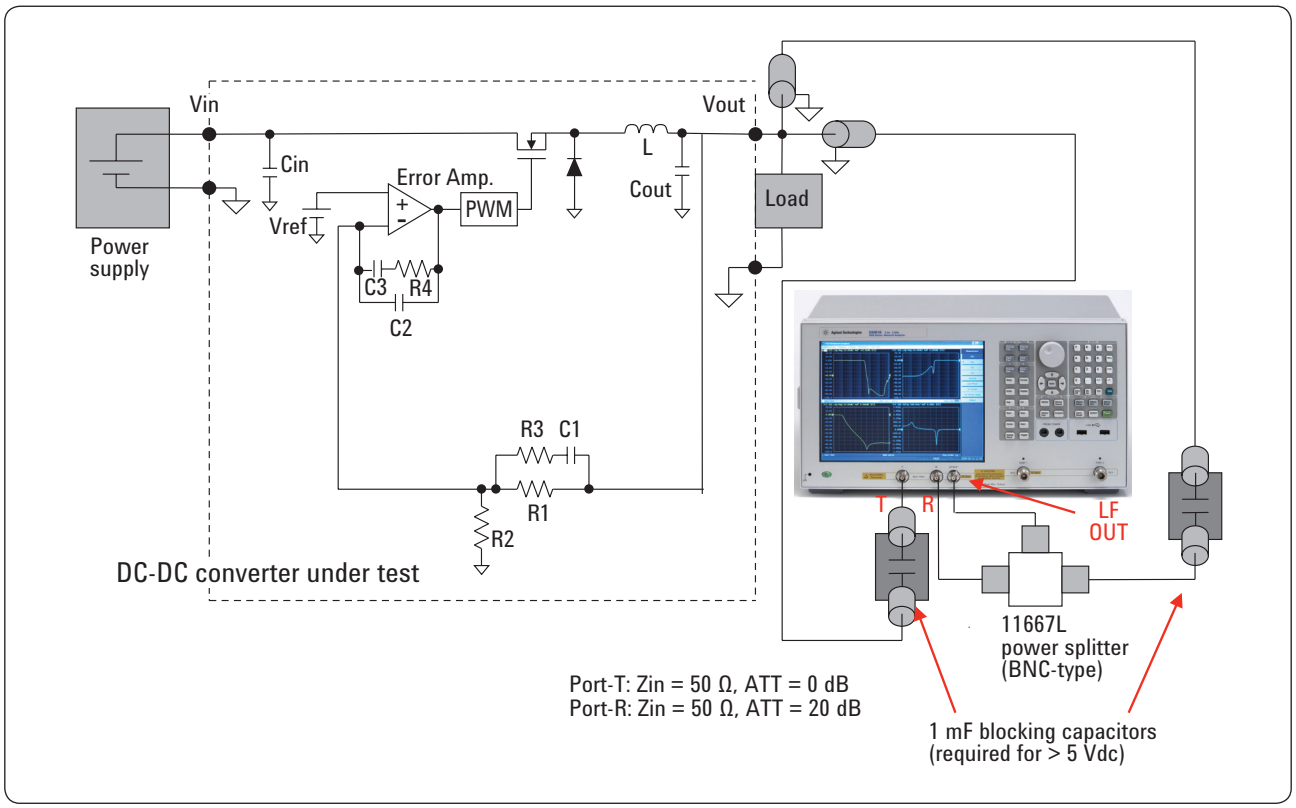


Figure 28. Configuration example of shunt-thru method

Configuration example of shunt-thru method, continued

To accurately measure the very small impedance of mΩ order with a minimal probing contact resistance, the measurement terminals should be contacted to the DUT with the 2-port probing [1] [2], and it is recommended that the measurement terminals are soldered to the DUT. If you combine two measurement terminals into one and contact the DUT with the 1-port probing, its lead length should be as short as possible, because its residual impedance will directly affect the mΩ impedance measurements.

Examples of the 2-port probing are illustrated in Figure 29. Two home-made probes are connected to the end of the test cables and the probes are contacted to the output terminal of the DUT. A home-made probe can be fabricated by utilizing a SMA receptacle (cutting off its three GND pins and using the remaining GND pin and the center pin for probing) or a SMA semi-rigid cable (cutting it short, stripping the center conductor, and soldering a short pin to the outer conductor).

When performing the thru calibration, make the thru condition whose electrical length is about the same as the total length of two probes.

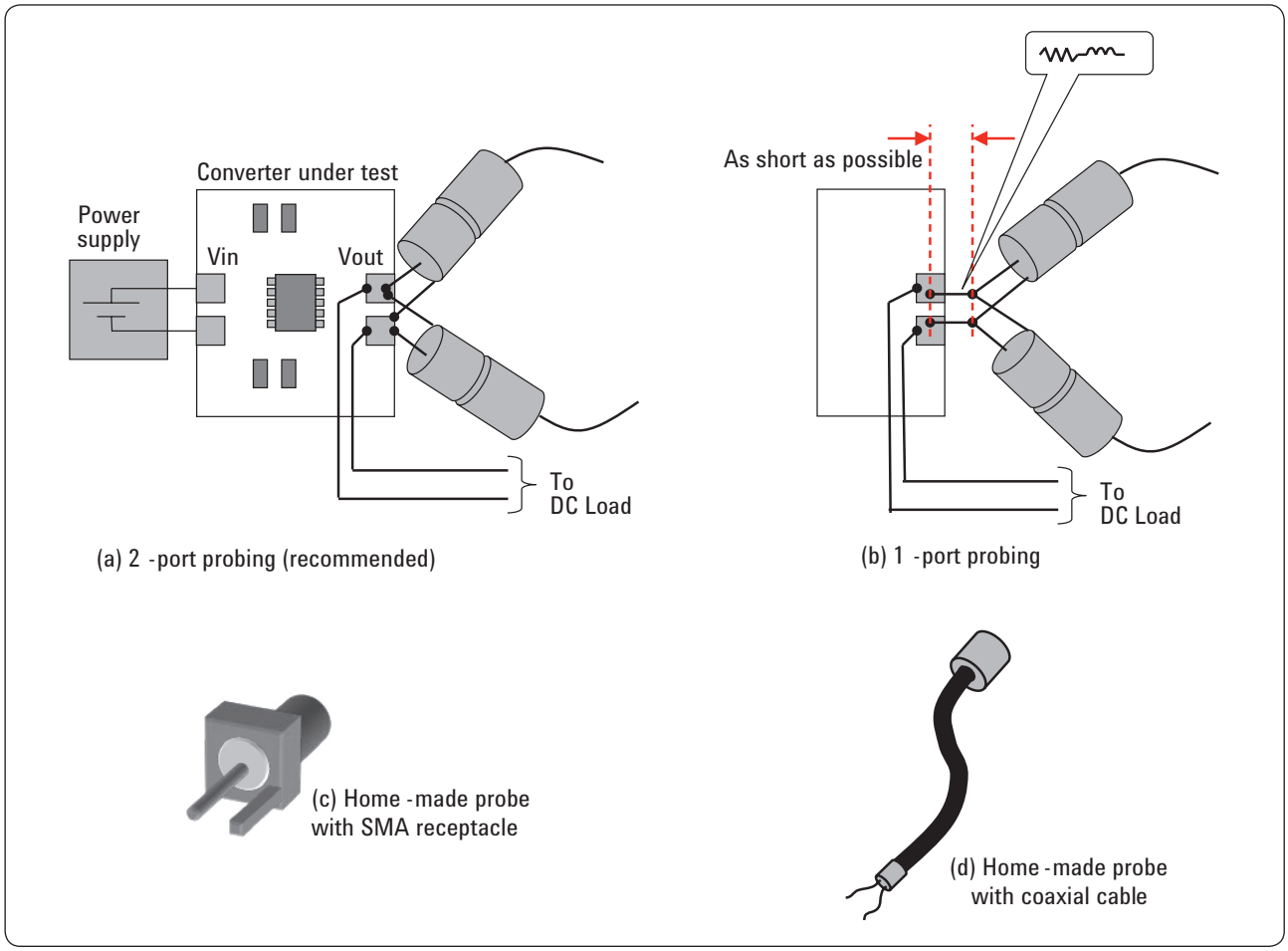


Figure 29. Example of probing method for shunt-thru method

Measurement example of DC-DC converter output impedance

Figure 30 and 31 show output impedance measurement examples of a 5 V-to-3.3 V DC-DC converter by using the shunt-thru method with the E5061B's gain-phase test port. The DUT is the same converter as that of the loop gain measurement example in the previous chapter. The measurement frequency range is from 10 Hz to 10 MHz. The IFBW is set to Auto/10 Hz-max. The port-T attenuator is set to 0 dB. The source level is set to 10 dBm during the measurement, and -5 dBm when performing the response through calibration.

NOTE: When turning the converter's power ON or OFF, it is recommended to temporarily change the port-T attenuator setting from 0 dB to 20 dB to avoid the receiver overload caused by the converter's transient output voltage. If the analyzer goes into the Overload Protection mode due to the transient voltage, you can recover it by pressing [System], (Overload Recovery), and (Clear Overload Protection) keys. The |Z| traces are plotted with the E5061B-005 impedance analysis function (Gain-phase shunt-thru method).

The left trace in Figure 30 is the |Z| measurement result when the converter and the electronic load are turned off. As you can see, the converter's off-state output impedance indicates a self-resonant impedance response of the converter's output capacitor. The right trace in Figure 30 is the |Z| measurement result under the 0.3 A load condition. As you can see, the |Z| trace in the low-frequency range is suppressed to about 2 mΩ with the converter's feedback loop operation. Thanks to the semi-floating receiver architecture of the gain-phase test port, the small impedance of mΩ order is correctly measured down to 10 Hz without being affected by the test cable ground loop.

Figure 31 shows the |Z| measurement traces under the 1 A and 2 A load conditions. As you can see, the DUT's impedance in the low-frequency range is higher than that of the 0.3 A load condition. In general, it is important to evaluate the output impedance under various load conditions and verify that the impedance is maintained under the target impedance and the impedance variation due to the load change is small.

Another important evaluation practice is to make sure the output impedance trace doesn't have a large positive peak as that could cause the transient noise under any load condition.

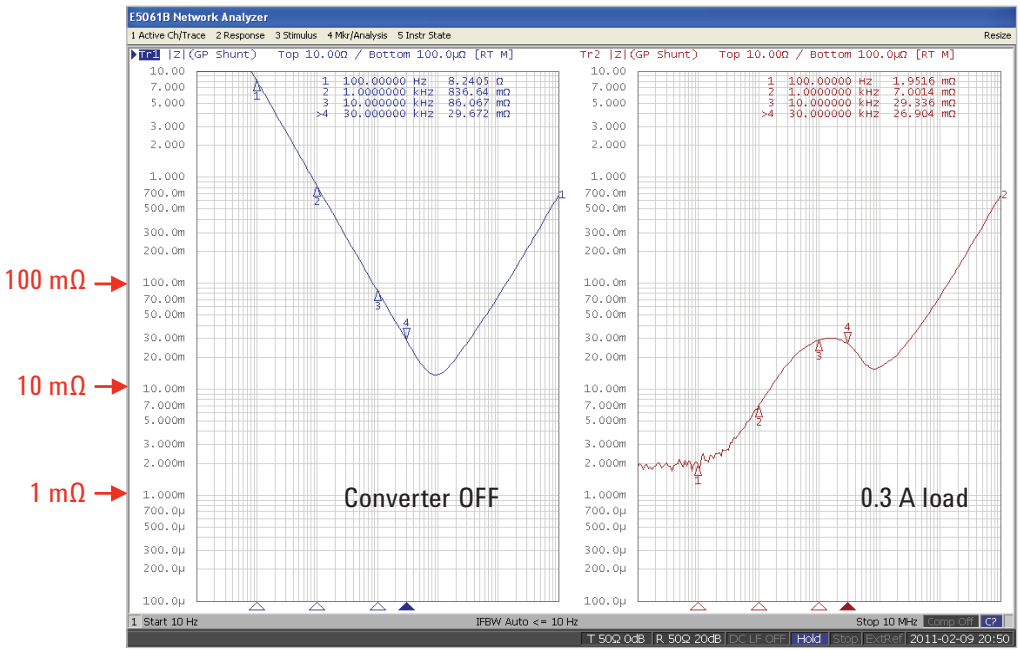


Figure 30. DC-DC converter output impedance measurement

Off-state and 0.3 A load conditions,
Start = 10 Hz, Stop = 10 MHz
Source = 10 dBm (-5 dBm at thru cal)
Port-T: ATT = 0 dB, Zin = 50 Ω, Port-R: ATT = 20 dB, Zin = 50 Ω

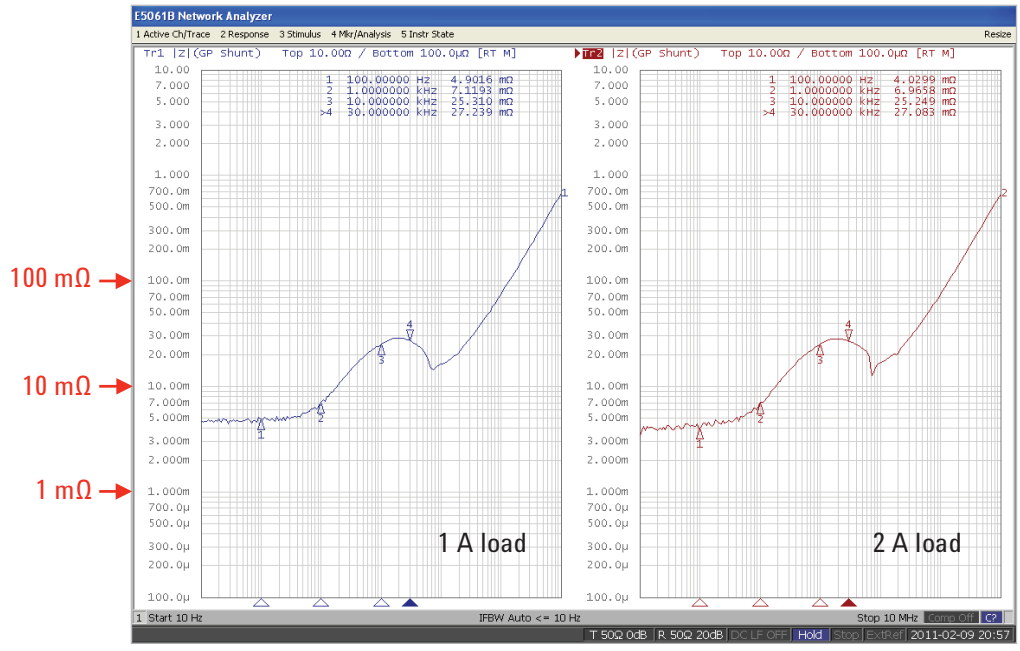


Figure 31. DC-DC converter output impedance measurement

1 A and 2 A load conditions,
Start = 10 Hz, Stop = 10 MHz
Source = 10 dBm (-5 dBm at thru cal)
Port-T: ATT = 0 dB, Zin = 50 Ω, Port-R: ATT = 20 dB, Zin = 50 Ω

Evaluating impedance of passive PDN components

Evaluating the impedance of passive components is an important task for designing the DC-DC converter's loop circuits and PDNs. The passive components mounted on the bare PCB power planes suppress the PDN impedance to a low value in the frequency range up to hundreds of MHz. The passive PDN components most commonly used are capacitors. Bulk capacitors such as electrolytic capacitors and high-dielectric MLCCs (multi-layer ceramic capacitors) are used as the output capacitors of the DC-DC converters, and also they act as the bypass capacitors that suppress the PDN impedance at higher frequencies beyond the converter's loop bandwidth. In addition, smaller bypass capacitors are mounted on the PCB to further suppress the impedance and resonance of the PDN up to higher frequencies.

Also, in some cases, ferrite beads or 3-terminal filters are mounted in series with the power path as decoupling devices for suppressing the noise that appears on the PDNs.

This section describes how to measure the impedance of bypass capacitors by using the E5061B with option 3L5 LF-RF network analyzer. In addition, a board-level impedance measurement example of populated PCB is shown.

For topics about other PDN components such as ferrite beads and inductors, refer to the document [3].

Impedance measurement methods with network analyzer

Figure 33 summarizes three major techniques for component impedance measurements with the network analyzer. Each method gives good measurement sensitivity at the impedance range where the measured AC voltage at the receiver V_T significantly varies. The shunt-thru method has good sensitivity in the small impedance range, and it is commonly used for measuring bypass capacitors which have small impedances down to the mΩ range around their series-resonant frequencies. On the other hand, for evaluating the components that have higher impedances, such as ferrite beads, the reflection method is a reasonable choice.

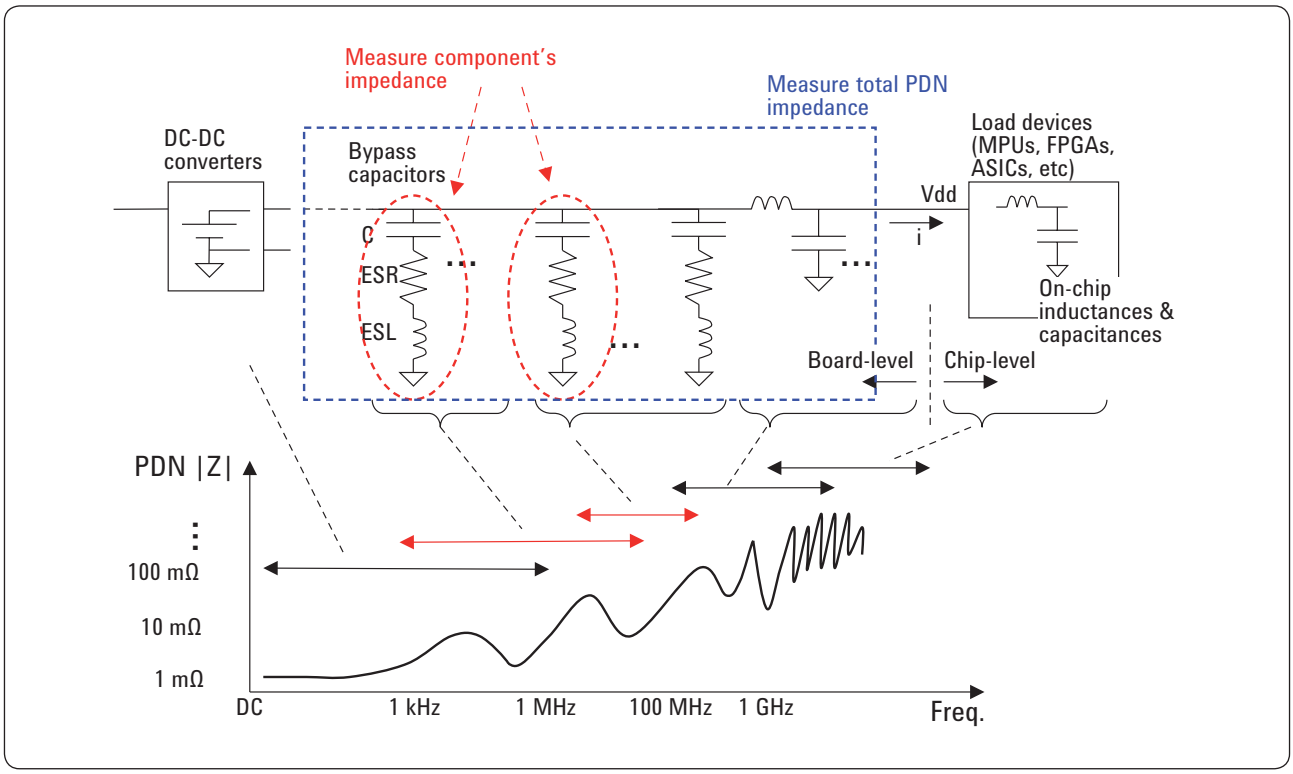
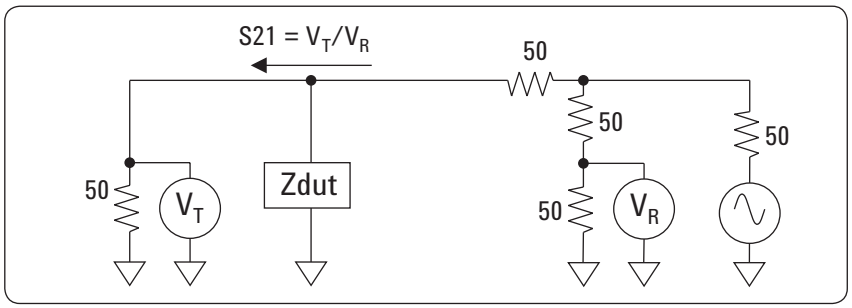
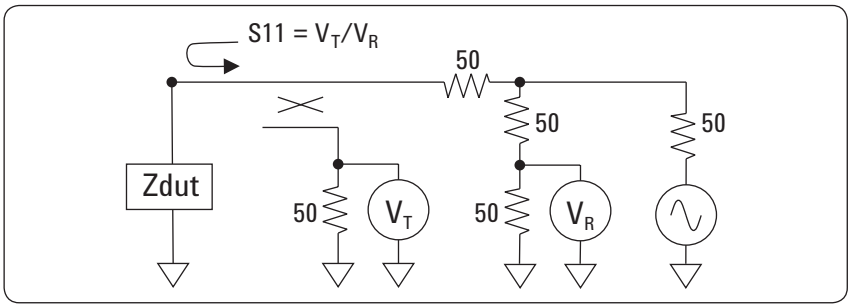


Figure 32. Passive component measurements in PDN

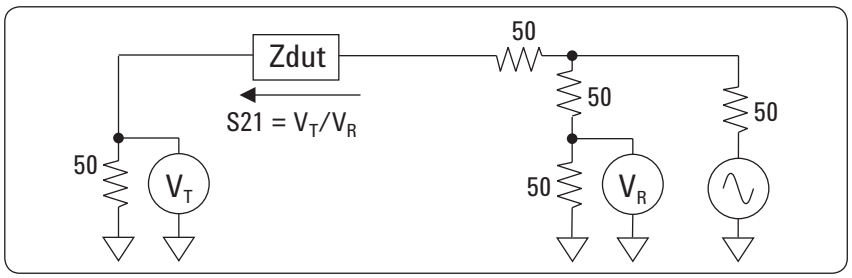


Shunt-thru method
For small impedance measurements
Zdut = 50 x S21/(2 x (1-S21))

(Configuration with 50 Ω R-ch receiver)



Reflection method
For middle impedance measurements
Zdut = 50 x (1+S11)/(1-S11)



Series-thru method
For large impedance measurements
Zdut = 50 x 2 x (1-S21)/S21

Note: Not applicable to grounded DUTs.

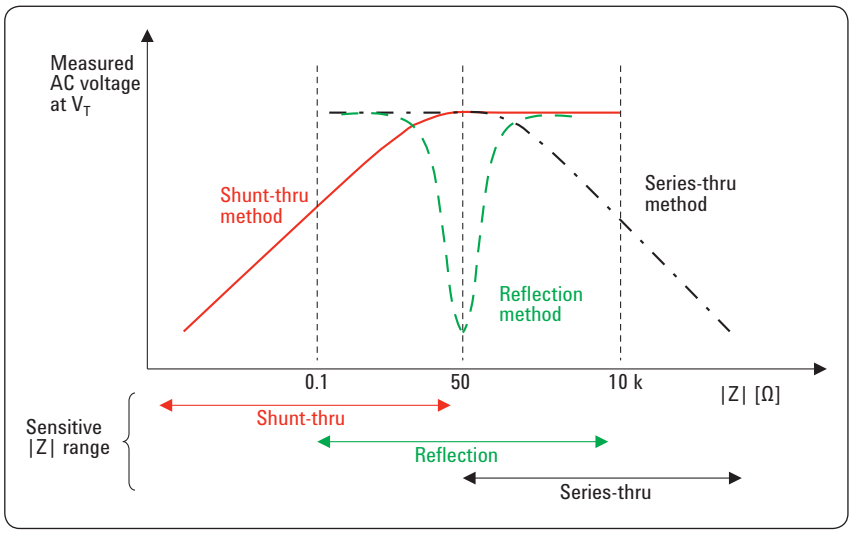


Figure 33. Impedance measurement methods with network analyzer

Configuration examples of shunt-thru method

Figure 34 shows a configuration example of the shunt-thru method for measuring bypass capacitors by using the E5061B's S-parameter test port. The DUT is mounted on a test board that has a 50 Ω co-planar transmission line. The S-parameter test port of the E5061B-3L5 covers 5 Hz to 3 GHz and you can measure the DUT's impedance characteristics across a broad frequency range.

For measurements up to 10 MHz, a simple response through calibration gives adequately good accuracy. For measurements up to hundreds of MHz or more, the 2-port full calibration should be performed at the coaxial planes to eliminate the impedance mismatch errors. The electrical length of the test board's 50 Ω transmission line should be compensated with the port extension.

Similarly to other network analyzers, the outer shield of the E5061B's S-parameter test port is connected to the analyzer's chassis ground, as described in the previous chapter. This may cause the impedance measurement error in the low-frequency range due to the source-to-receiver test cable ground loop when the DUT has a very large capacitance of millifarad order.

To avoid this measurement error, magnetic cores should be attached to the test cable, as illustrated in Figure 19 and 20. Or, if the test frequency is below 30 MHz, you can avoid this measurement error by using the gain-phase test port, which has semi-floating receiver architecture as described in the previous chapter. Figure 35 shows a configuration example.

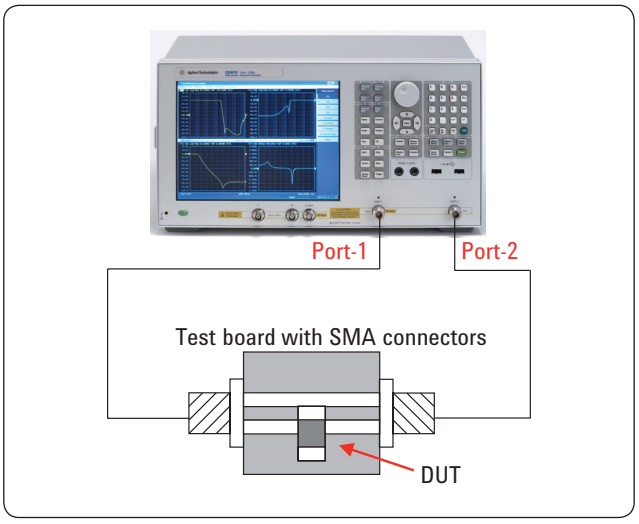


Figure 34. Shunt-thru method with S-parameter test port

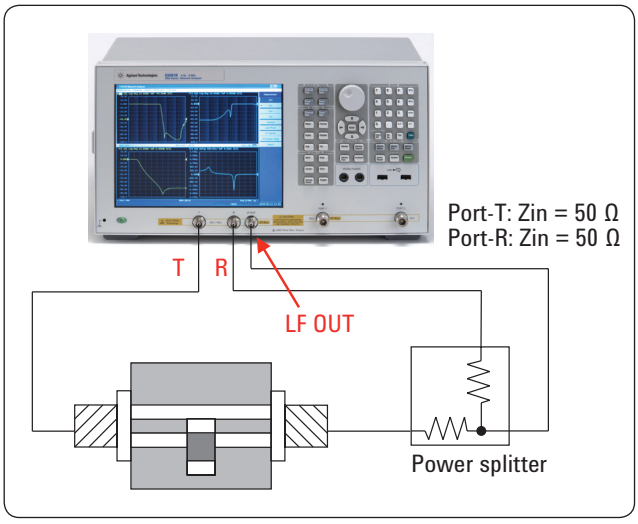


Figure 35. Shunt-thru method with gain-phase test port

DC voltage biased measurement for MLCC

Large-capacitance MLCCs with high dielectric constant have DC voltage dependence. To accurately evaluate the MLCCs under the conditions similar to the actual PDNs, it is preferable to measure their impedance with the DC voltage bias applied. The built-in DC bias source of the E5061B-3L5 allows you to easily perform DC-voltage biased measurements for MLCCs from the low-frequency range. Figure 36 shows an example of the DC-biased measurement configuration by using the gain-phase test port.

Basically, the configuration is similar to the shunt-thru method shown in Figure 35, but the receiver ports R and T are set to the high impedance input mode for measuring the DC-biased DUT. The AC voltage across the DUT is measured with the port T, and the AC current flowing through the DUT is measured by sensing the AC voltage across the resistor Ri with the ports R and T. By performing the 3-term calibration (OPEN/SHORT/LOAD calibration) in the impedance domain, the measurement system is fully adjusted at the measurement terminal on the test board and the DUT's impedance can be directly indicated on the screen, without the need for considering the equation for converting the raw T/R measurement data into the impedance.

The 3-term calibration in the impedance domain can be executed by performing the 1-port full calibration for the raw T/R measurement and converting the measured data to the impedance with the reflection impedance conversion. (Be careful not to use the shunt-thru impedance conversion in this case, although the physical connection is the shunt-thru.)

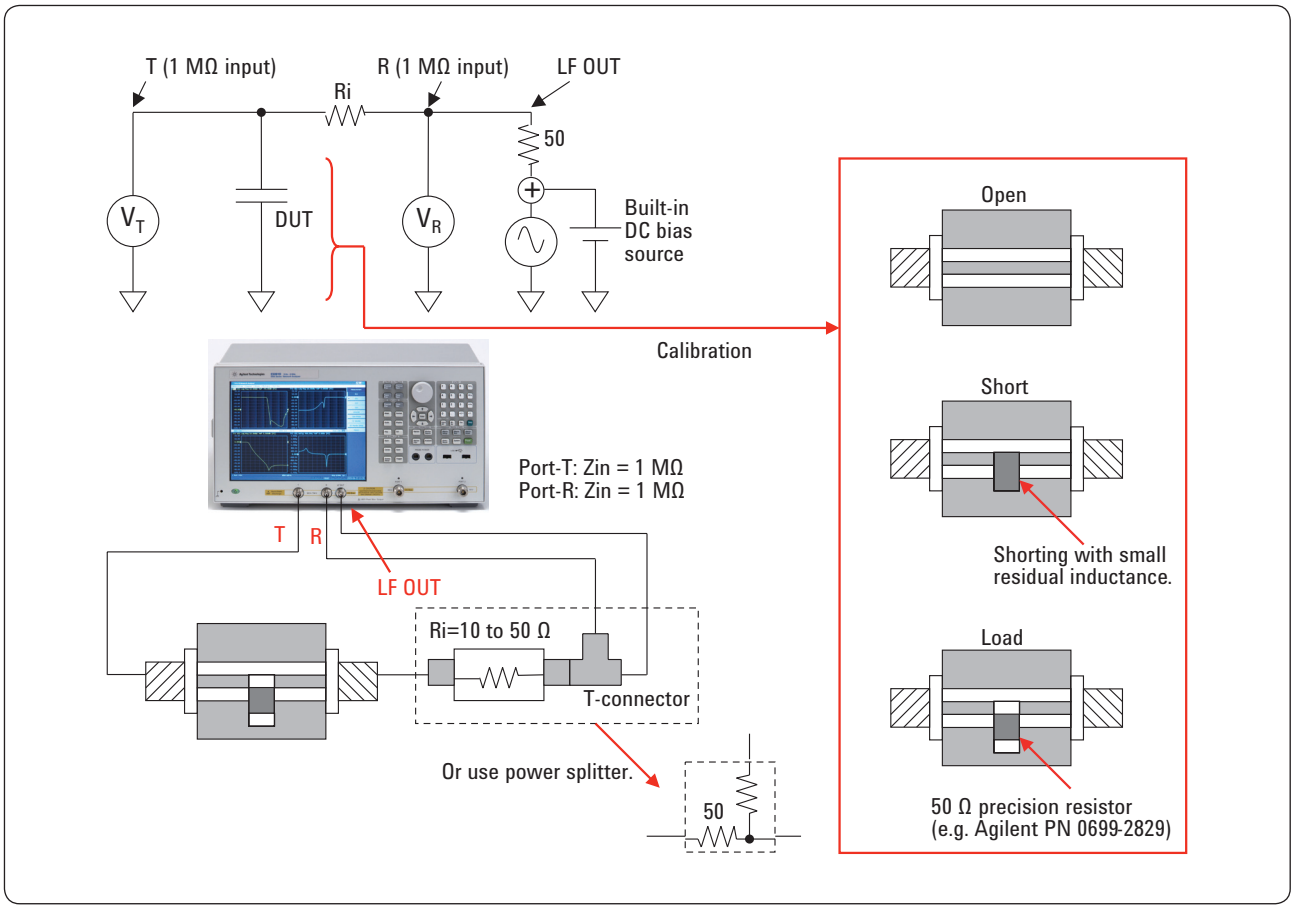


Figure 36. Configuration example of DC voltage biased MLCC measurements

Measurement example of MLCC

Figure 37 shows an impedance measurement example of a large-capacitance MLCC with the S-parameter test port of the E5061B-3L5. The DUT is mounted on the test board as shown in Figure 34. The test frequency range is 100 Hz to 1 GHz. The 2-port full calibration is performed at the end of test cables and the transmission lines on the test board are compensated with the port extension. The impedance magnitude |Z|, phase, capacitance Cs, and inductance Ls are plotted with the E5061B-005 impedance analysis function (Port 1-2 shunt-thru method).

Figure 38 shows a measurement example of the same MLCC by using the gain-phase test port. The measurement configuration is the one shown in Figure 36. Note that the input impedance of R and T ports must be set to 1 MΩ after setting the measurement mode to gain-phase shunt-thru and selecting all impedance parameters to be measured. The test frequency range is 100 Hz to 10 MHz. The 3-term calibration is performed by using the Impedance Calibration function and the open/short/load calibration devices, like the examples shown in Figure 36. As indicated with the marker reading, the capacitance measurement result at 10 kHz is about 47 uF.

On the other hand, Figure 39 shows the measurement result by applying the DC bias of 3 Vdc in the same measurement configuration. As you can see, the capacitance at 10 kHz is significantly decreased to 29 uF due to the DUT's DC voltage dependence. This indicates the importance of evaluating the large-capacitance MLCCs under the DC biased condition similar to the actual PDN condition.

The large-capacitance MLCCs also have a dependence on the AC voltage level. If necessary, check the AC voltage level actually applied to the DUT at the frequency point you are interested. For example, in the configuration of Figure 36, the AC voltage level applied to the DUT can be calculated as;

Vdut = Vsrc x Zdut/(Zdut + 50 + Ri)
Vsrc = 2 x SQRT (50 x 0.001 x
10^(Pset/10)

where Pset is the source power setting in dBm, Ri is the current sensing resistor shown in Figure 36, and Zdut is the DUT's impedance which is approximately calculated as 1/(2*pi*f*C).

Also, it is possible to apply a constant AC voltage level to the MLCC by adjusting the source setting point-by-point with the segment sweep capability [3].

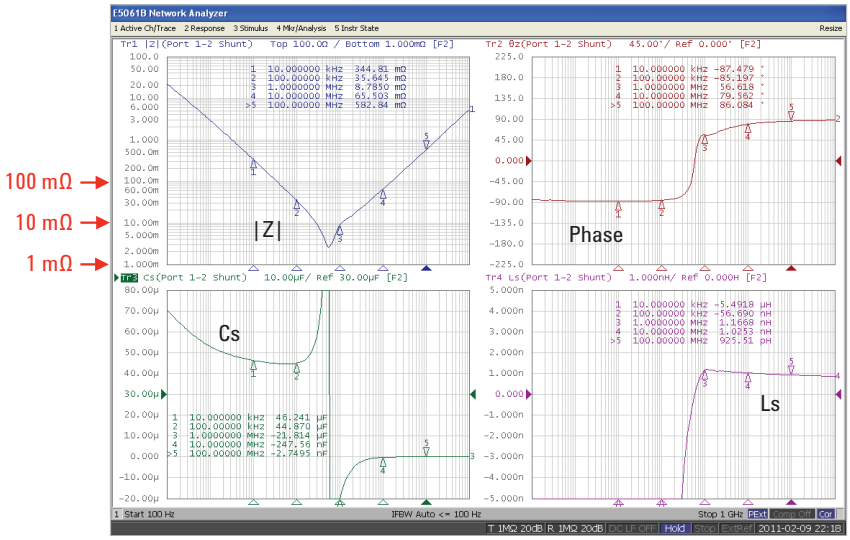


Figure 37. MLCC impedance measurement example

S-parameter test port (Port 1-2 shunt-thru method)
Start = 100 Hz, Stop = 1 GHz
Source = 0 dBm, IFBW = Auto/100 Hz-limit

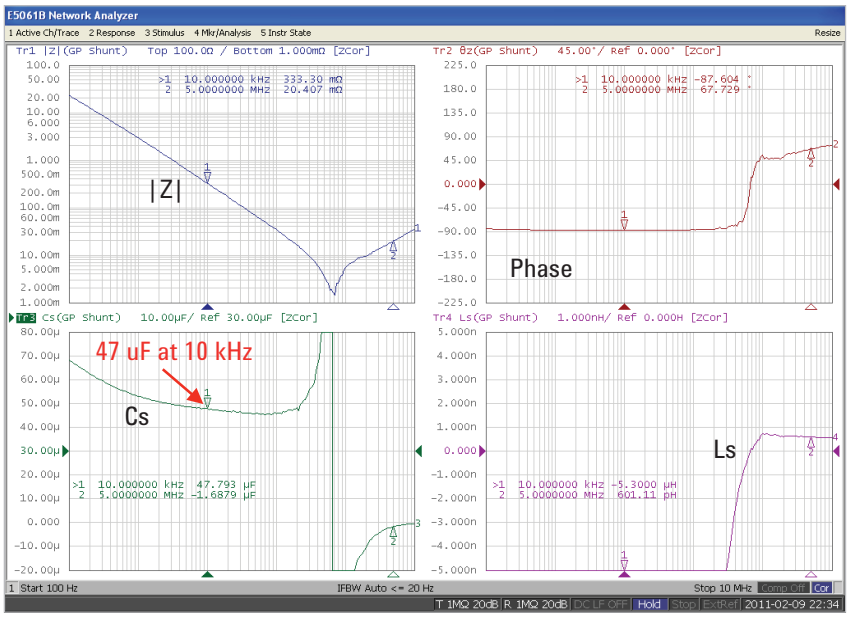


Figure 38. MLCC impedance measurement example (without DC bias)

Gain-phase test port (Gain-phase shunt-thru method)
Start = 100 Hz, Stop = 10 MHz
Source = 0 dBm, IFBW = Auto/20 Hz-limit
Port-T & R: ATT = 20 dB, Zin = 1 MΩ

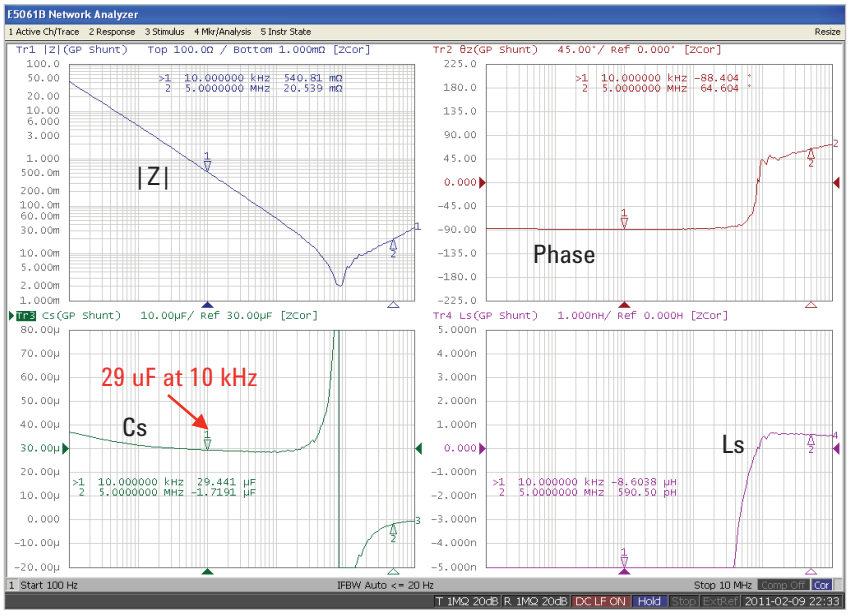


Figure 39. MLCC impedance measurement example (with 3 V DC bias)

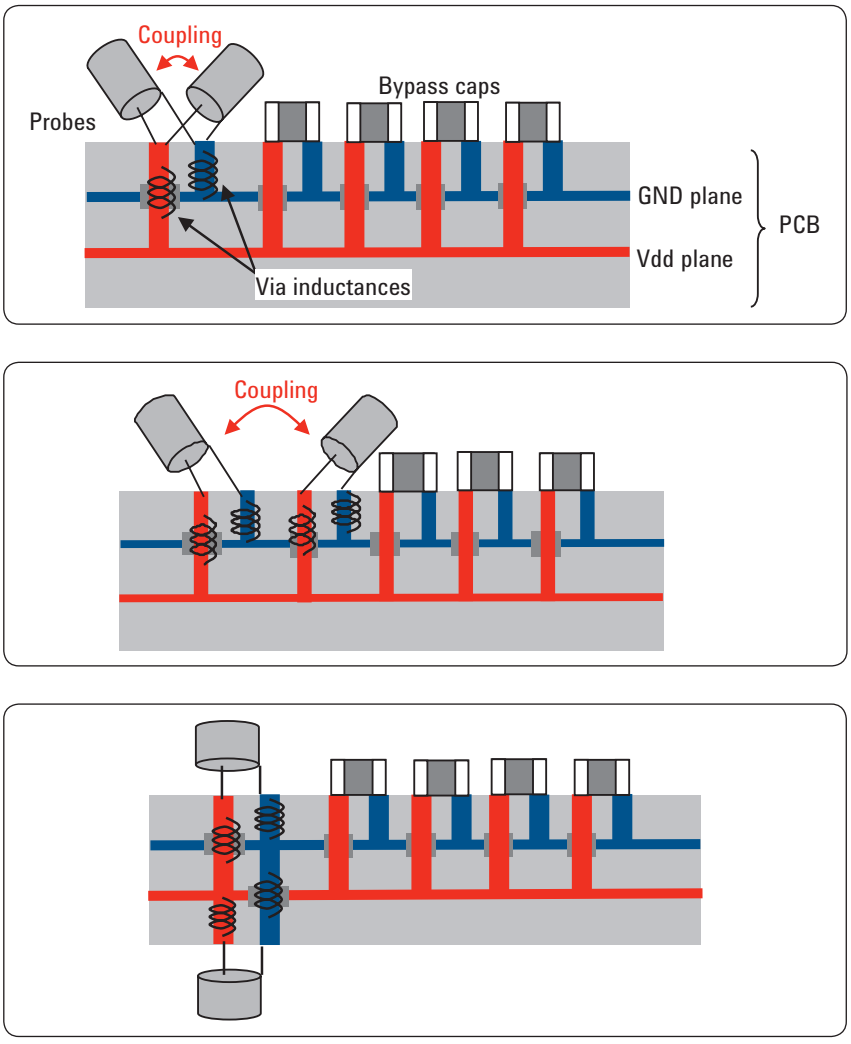
Gain-phase test port (Gain-phase shunt-thru method)
Start = 100 Hz, Stop = 10 MHz
Source = 0 dBm, IFBW = Auto/20 Hz-limit
Port-T & R: ATT = 20 dB, Zin = 1 MΩ

Measuring PCB populated with bypass capacitors [1]

The next measurement example is a board-level PDN self-impedance measurement of a PCB populated with bypass capacitors. With this measurement, we can verify that the bypass capacitors suppress the PDN impedance to a targeted value. Figure 40 compares three different 2-port probing methods. The method shown in Figure 40 (c) is the best way to measure a very small self-impedance between the power and ground planes of the populated PCB up to the high-frequency range, where the total inductance of the bypass capacitors and the PCB itself is the dominant part of the impedance. By contacting two probes from opposite sides of the board like Figure 40 (c), we can minimize the mutual coupling inductance between two probes, and also via inductances will not be included in the measurement result of the plane-to-plane impedance.

To minimize the probe coupling error when probing from the same side of the board, the current loop area formed by the probe's center and ground pins should be as small as possible, and also the distance between the probes should be as far as possible. However, when measuring the self-impedance with the method shown in Figure 40 (b), it should be noted that the distance between two probing positions must be sufficiently smaller than the wavelength of the maximum test frequency of interest.

For further details about the probing techniques, refer to document [1].



(a) Probing from the same side at one pad pair

- Affected by the probe coupling residual inductance.
- Via inductances will be included in the measured value.

(b) Probing from the same side at adjacent pads

- Affected by the probe coupling residual inductance.
- Via inductances will not included in the measured value.

(c) Probing from opposite sides at through-hole pads

- Probe coupling residual inductance will be minimal.
- Via inductances will not be included in the measured value.

Figure 40. Summary of 2-port probing methods for PCB

Measurement example of PC motherboard

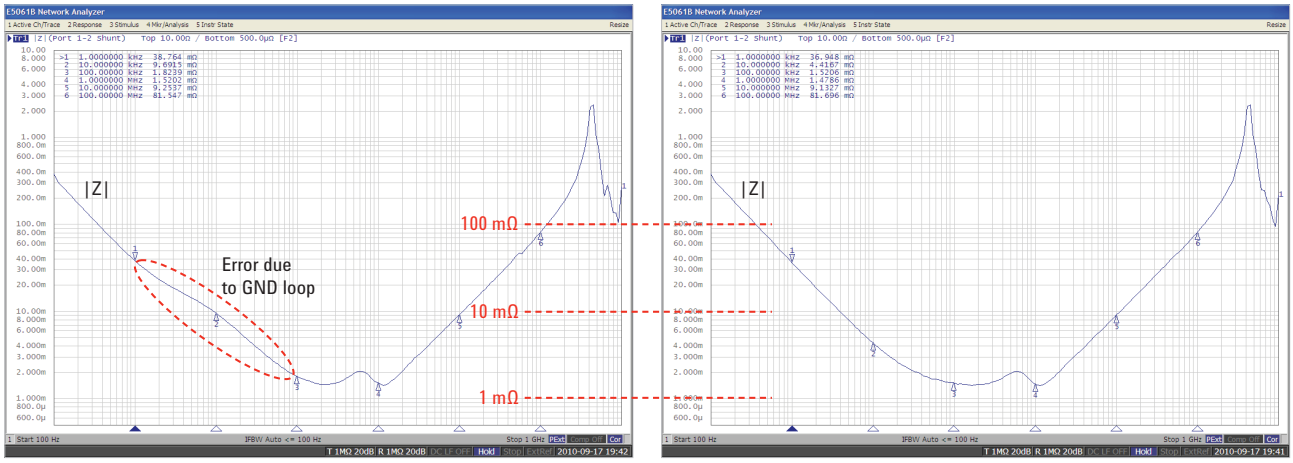
Figure 41 shows a measurement example of a PC motherboard populated with plenty of bulk capacitors and small capacitors. The power of the motherboard is turned off, and we measure the total self-impedance between the power and ground planes which consists of the bypass capacitors and the bare PCB's impedance characteristics. Since the board of this example has no test pads, one of bulk bypass capacitors mounted on the through hole is removed and home-made probes (made with SMA receptacles) are soldered to the pads from the top and bottom sides of the board.

The 2-port full calibration is performed at the end of the coaxial test cables, and the electrical lengths of the probe heads are compensated by using the port extension The swept frequency range is from 100 Hz to 1 GHz, but the frequency range concerned in this measurement example is mainly kHz to hundreds of MHz range, where the on-board bypass capacitors suppress the PDN impedance. (The maximum frequency range of interest depends on the applications.)

The Figure 41 (a) is the measurement result without attaching a magnetic core to the test cable. As the mounted bulk capacitors provide a small impedance in the low-frequency range, the measurement error due to the test cable ground loop appears in the low-frequency range.

On the other hand, Figure 41 (b) is the measurement result by attaching a large toroidal core to the test cable. Thanks to the effect of the core, the impedance is accurately measured down to the low-frequency range.

In this measurement example, the PDN impedance from low- to high-frequencies is evaluated with a single swept measurement by using the E5061B's S-parameter test port and the external magnetic core. But if you do not have an appropriate magnetic core, it is recommended to separately perform a low-frequency measurement by using the gain-phase test port and a high-frequency measurement by using the S-parameter test port.



(a) Without magnetic core

(b) With magnetic core

Figure 41. Measurement example of PCB populated with bypass capacitorsS

S-parameter test port (port 1-2 shunt-thru method)
Start = 100 Hz, Stop = 1 GHz
Source = 10 dBm, IFBW = Auto/100 Hz-limit

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References

[1] "Frequency Domain Characterization of Power Distribution Networks", Istvan Novak, Jason R. Miller (2007, Artech House)

[2] "Frequency-Domain Power-Distribution Measurements –An Overview", Istvan Novak (DesignCon East 2003, June 2003)

[3] "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range", Istvan Novak, Yasuhiro Mori, Mike Resso(DesignCon 2010, Feb.2010)

[4] "Spectrum and Network Measurements", Robert A. Witte, 1993

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